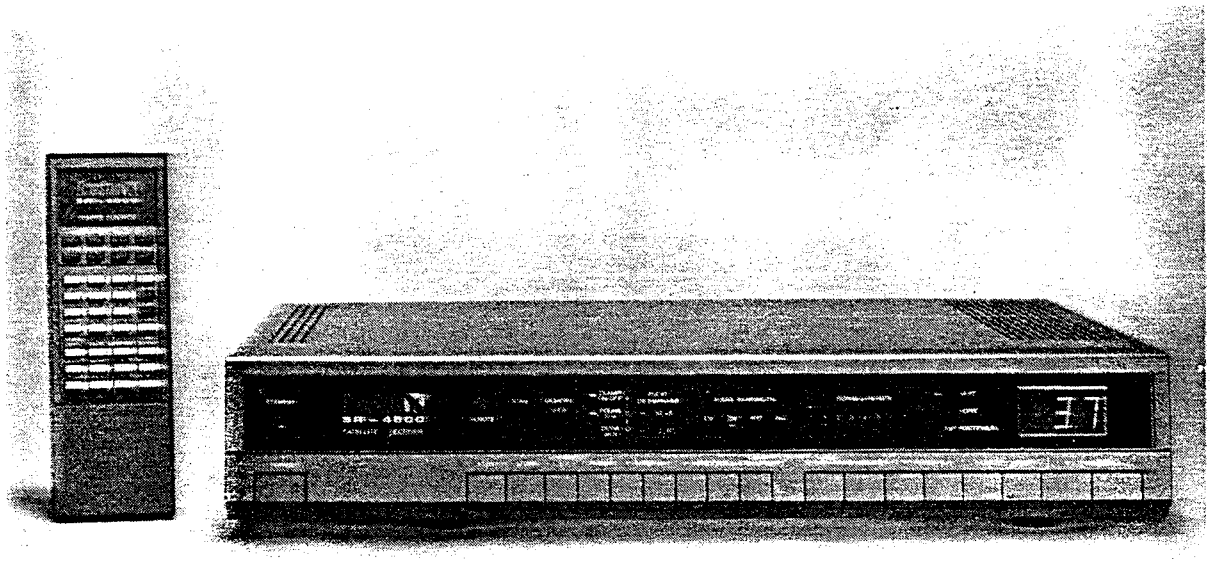
ECHOSTAR SR-4500

Integrated Satellite Receiver and Antenna Positioner



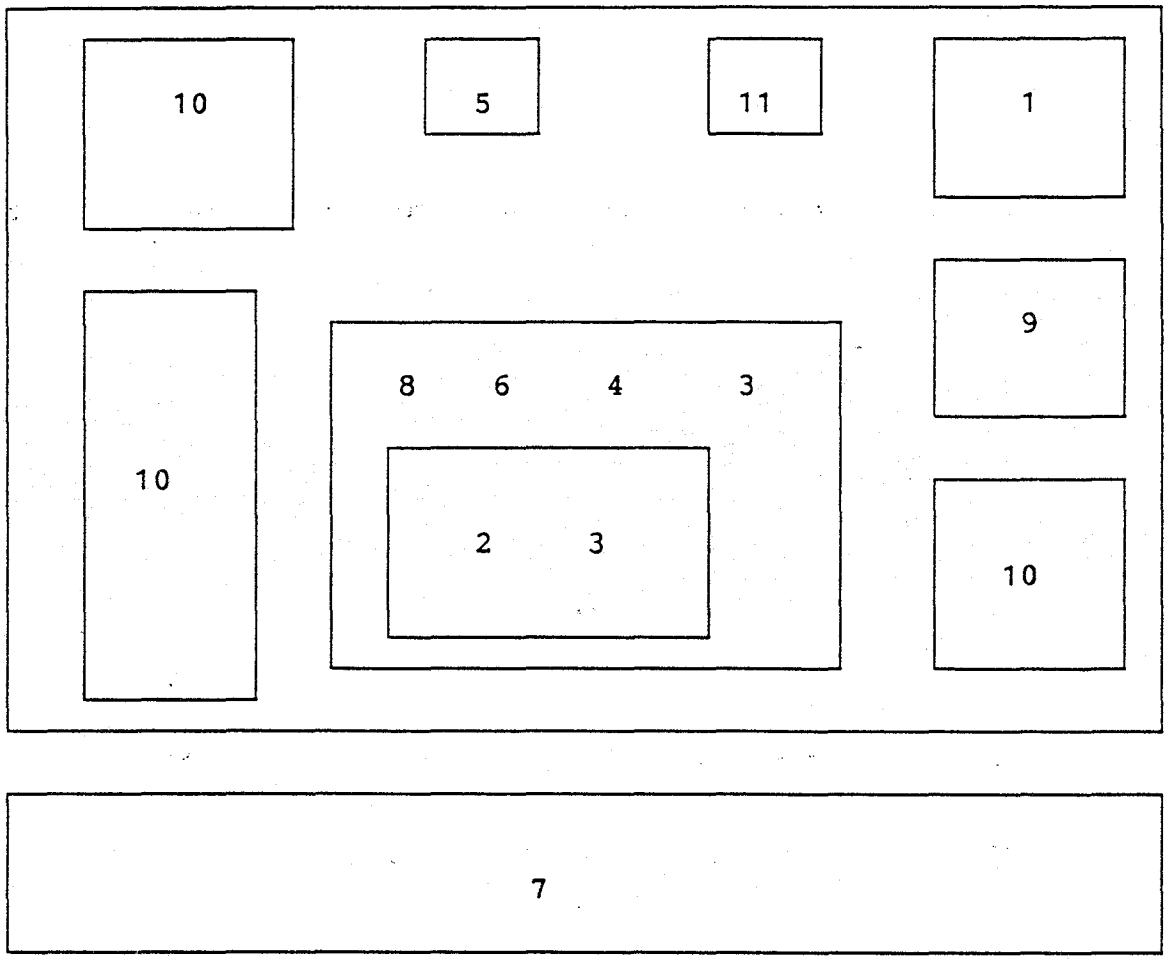
Technical Manual

The ECHOSTAR SR-4500 SATELLITE RECEIVER/POSITIONER

The *ECHOSTAR* SR-4500 is a very versatile and modular-built satellite receiver. Eight components take care of the primary functions: there are 11 main circuits.

1. First downconvertor (tuner)
2. Demodulator (RF -> baseband)
3. Video processing
4. Audio processing
5. RF modulator (UHF)
6. Microprocessor controller
7. Front panel controller
8. Polarotor circuit
9. Actuator circuit (positioner)
10. Power supply (linear)
11. MAC-preamplifier

The physical layout looks like this:



GENERAL CIRCUIT DESCRIPTION

1. **First downconvertor (tuner)**

   This tuner has a frequency input range of 950 - 1750 MHz (those are the LNB output frequencies). The tuner is based on the PLL synthesizer principle. Since there are 50 channels in FSS and 40 in DBS mode, this means that frequency steps are 16 resp. 20 MHz.

   The synthesizer is based upon the 145155 (Motorola), a low power CMOS device that contains (almost) all circuits needed for a frequency synthesizer.

   The tuner converts the initial input range to an IF of 479.5 MHz. A second downconvertor (based upon a diode mixer) changes this into the 70 MHz output. Both convertors were fitted on one PCB.

2. **Demodulator**

   The demodulator converts the IF-signals into
   - base band video
   - AGC signal

   Video bandwidth (deviation) can be selected. The signal strength is proportional to the AGC voltage (reciprocal).

3. **Video processing**

   This circuit converts the baseband video signal into clamped / unclamped, inverted / uninverted video signal. All these features are software selectable. It also has a composite baseband output, that can be used with decoders (Filmnet, BBC, etc.) or MAC-decoders.

4. **Audio processing**

   The audio circuit is also synthesised; another PLL circuit enables tuning steps of 10 kHz. Bandwidth is selectable (130, 280, 400, 900 kHz), as is de-emphasis (50, 75µs and J17, which is a CCIR standard).
   Volume and mute (lowest volume level) control the audio level on both line and RF output.

5. **RF modulator**

   This module generates a PAL RF signal (adjustable from UHF channel 30 - 40), both audio and video modulated.

6. **Microprocessor circuit**

   This circuit is composed around the well known Intel 8085. The standard configuration consists of memory and some I/O parts. The microprocessor translates frontpanel commands (issued by the buttons on the frontpanel or by the handheld) into the appropriate electronic actions.

7. **Frontpanel controller**

   All frontpanel functions are converted into a digital (8 bits) format, so that the microprocessor can understand, what actions it is supposed to undertake. The frontpanel also displays all relevant information, like channel number, audio / video parameters, signal strength etc.

8. **Polarotor circuit**

   The polarotor circuit is nothing but a pulse width modulator, controlled by the microprocessor circuits. It causes the polarotor to move in steps of 5 degrees in both horizontal and vertical direction.

9. **Actuator (positioner) circuit**

   This circuit controls movement of the actuator in eastern and western direction. A pulsed signal from the actuator itself protects it from mechanical defects.

10. **Power supply**

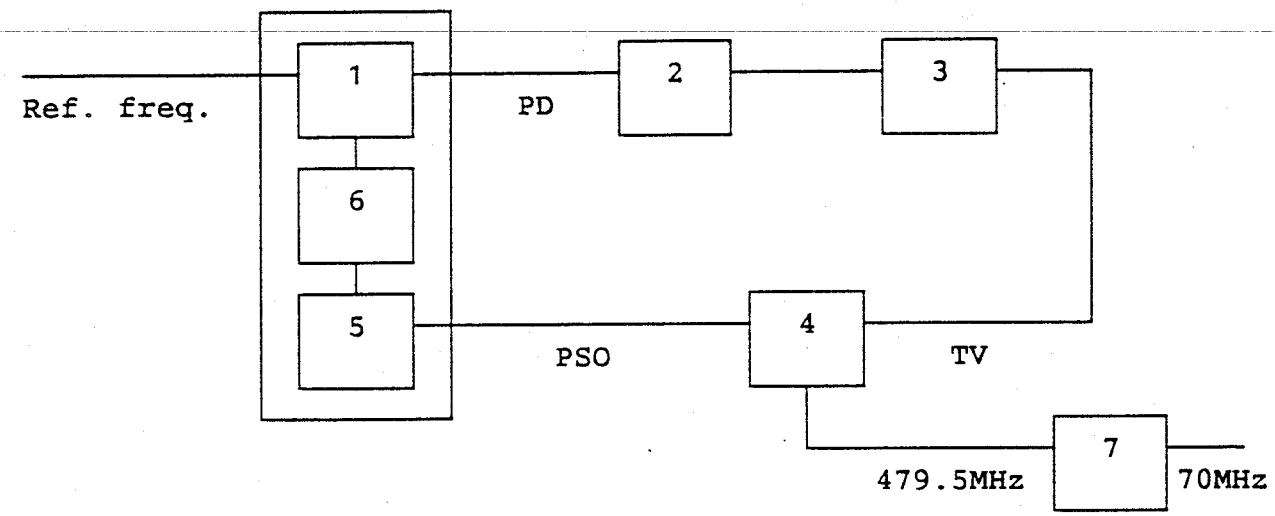
    This circuit generates all the required voltages for both internal and external modules (ie. LNB's).

11. **MAC-preamplifier**

    This small circuit prepares the video-signal to be fed into a MAC-decoder. The decoder output signal is unclamped, unfiltered and non-de-emphasized.

Circuit analysis

1. First Downconvertor (tuner)



Functional diagram

1. phase detector (U201)
2. low pass filter (U202)
3. buffer (U202)
4. tuner (output 479.5 MHz) UTI
5. prescaler (U201)
6. divider programmable (U201)

The main circuit is U201, the micropower CMOS IC 145155. This IC contains almost everything to make a frequency synthesizer.

The difference in reference frequency and divided tuner output frequency is proportional to the tuning voltage (pin 6, U201). This voltage (a triangular shaped wave form) is filtered through U202a and U202b (2nd order low pass filter). Then it is fed into the tuner varactor input (tuning input).

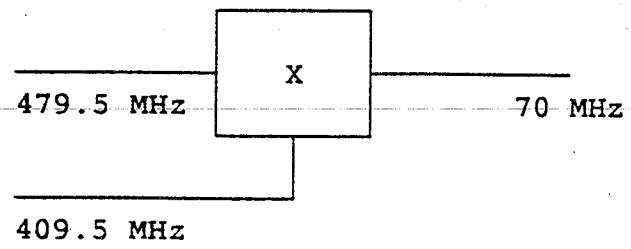
Table 1 gives the typical tuning voltage versus-input frequency. Diagram 1 is the first down-convertor stage.

Table 1 : Channel versus tuning voltage

Chan.	Freq.	Tv	Chan.	Freq.	Tv	Chan.	Freq.	Tv
1	958	1.89	18	1230	6.98	35	1502	11.76
2	974	2.12	19	1246	7.29	36	1518	12.00
3	990	1.36	20	1262	7.59	37	1534	12.24
4	1006	2.61	21	1278	7.90	38	1550	12.48
5	1022	2.89	22	1294	8.30	39	1566	12.74
6	1038	3.17	23	1310	8.50	40	1582	13.02
7	1054	3.48	24	1326	8.80	41	1598	13.32
8	1070	3.79	25	1342	9.10	42	1614	13.62
9	1086	4.11	26	1358	9.38	43	1630	13.92
10	1102	4.43	27	1374	9.66	44	1646	14.24
11	1118	4.75	28	1390	9.94	45	1662	14.58
12	1134	5.07	29	1406	10.22	46	1678	14.93
13	1150	5.39	30	1422	10.49	47	1694	15.29
14	1166	5.72	31	1438	10.75	48	1710	15.67
15	1182	6.04	32	1454	11.01	49	1726	16.06
16	1198	6.32	33	1470	11.27	50	1742	16.47
17	1214	6.67	34	1486	11.52			

Ch = Channel (in FSS mode)
Freq = frequency, in MHz
Tv = tuning voltage, in volt (DC) (tolerance 2%)

The tuner's output frequency at 479.5 MHz is converted down to 70 MHz, the final IF frequency.



Functional diagram

The diode-mixer, made up of D1-D4, mixes the input frequency of 479.5 MHz with a local oscillator signal of 409.5 MHz. This results in an output frequency of 70 MHz.

The circuitry around L1, L2, L3 is a bandfilter (typ. 479.5 MHz).
The local oscillator (LO) is made up of Q1 and Q2's function is that of a level amplifier with a 70 MHz output filter.

Diagram 2 represents the second down-convertor.

2. Demodulator

The demodulator is nothing but an IF-amplifier, operating at 70 MHz.
It converts the wideband FM-modulated composite signal into an AM baseband signal, from which both audio and video are extracted.
Two filters are responsible for the IF-bandwidth. These filters are of the so-called "SAWF" (Surface Acoustic Wave Filter) type, or F101 and F102 in diagram 3.
F102 is the wideband , F101 is the narrow-band filter.
Bandwidth is software controlled (by the so-called "video- deviation" function); Q104, 105 and 106 perform the actual switching.
Q107, 108, 109 adjust the level (small signal amplifiers) of the signal, which is fed into the complex FM-demodulator.
This FM-demodulator consists of U103 (MC10216) and U104 (MC1496). The very complex IC U104 (a double-balanced mixer) generates the AM video signal.
Q111 and 113 are video-amplifiers: VR101 can be adjusted for 1.1 Vpp (when a standard PAL signal is applied to the receiver's input) on pin 4 of connector P104.
Q112 is an emitter follower, buffering the base-band signal. U105 (LM358) is the AGC-amplifier; VR102 adjusts the minimum AGC-level (adjust it for a minimum of sparklies in the video) and VR103 adjusts the (relative !) field strength readout.

Diagram 3 represents the demodulator circuit.

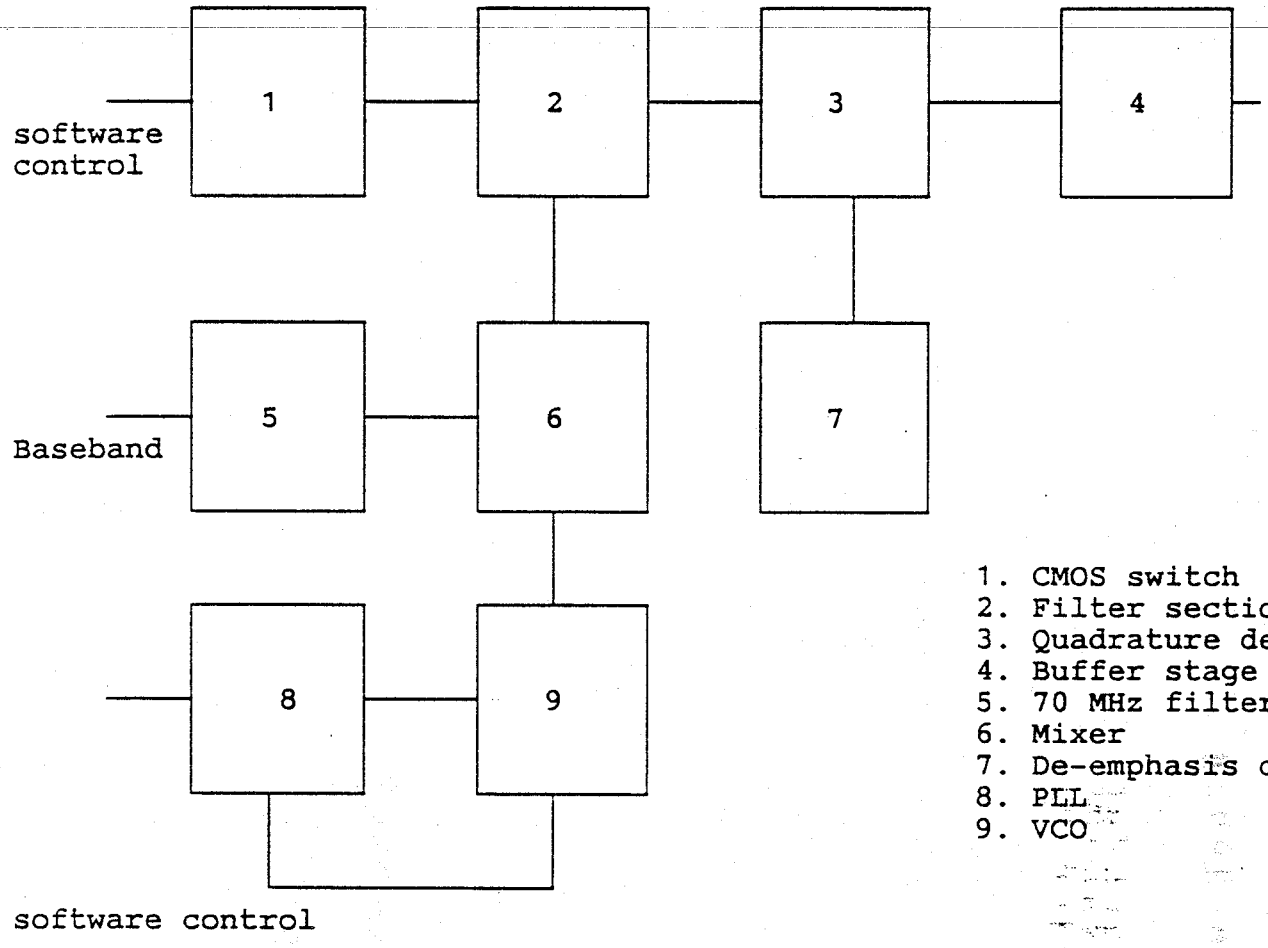
3. Video Processing

The video processing circuits convert the baseband video into a clamped / unclamped, inverted / non-inverted signal. It also switches the narrow or wideband (demodulated) video.
The unprocessed video is fed into Q1 (emitter follower); The circuit composed around L2, R6, 7, 8 and C4, 5 is a bandfilter. Then the buffered signal is applied to a differential amplifier, made up of Q2, 3 and Q4. Q4 is a current-mirror, needed for a correct operation of the differential amplifier.
The collector of Q3 delivers the normal video (positive), whereas the collector of Q2 carries the inverted (negative) video. An electronic switch (K1, Q5) switches between the two polarities.
Q6, 7 and 8 form buffer stages (all emitter followers); the signal is filtered (bandfilter consists of L4, C16, 17) before it can be called: "baseband video".
Buffer Q9 feeds the inverted / non-inverted video into video filters, FL1 or FL2 (electronically switched), before it goes into a second differential amplifier.
This differential amplifier, which adjusts the video for the correct clamping level, consists of Q10 and Q11; R41 is the (passive) current-mirror. The line-output level (1.0 Vpp, when a standard PAL test signal is applied to the receiver's input) can be adjusted with VR2.

Clamping or unclamping is software selected by an electronic switch (K3, Q17).
Q12, another emitter-follower, feeds the buffer stage, made up of Q14, 15 and Q16 after which it is filtered (L7, C32, 33).
The result is a standard PAL video signal, fed into the RF (UHF) modulator and the video line-output.

Diagram 4 represents the video processing circuits.

4. Audio processing



1. CMOS switch
2. Filter section
3. Quadrature detector
4. Buffer stage
5. 70 MHz filter
6. Mixer
7. De-emphasis control
8. PLL
9. VCO

Functional diagram

Although the audio processing looks very complicated, there are only 3 main sections.
I.Bandwidth selector; selects one of four available bandwidths (130, 280, 400, 900 kHz).
II.Sound carrier frequency synthesizer
III.Quadrature detector with selectable de-emphasis

A buffer stage feeds both line output and the RF modulator audio input.

The bandwidth is software controlled by U19 (CMos switch, 4052). It selects one of four ceramic filters (from the 10.7 MHz series). Diode switching selects a particular filter (Diodes CR5 - 12).

The baseband signal is filtered by a thick film circuit, FL3 (BP-70E). Transistor Q18 is a level (inverting) amplifier, passing the filtered signal to Q19. This dual gate Mosfet functions as a low-level mixer. It mixes the modulated audio with a signal (variable frequency) generated by a PLL circuit. This PLL circuit consists of U2 (MC145155, the chip that contains all PLL components), U8 (LM358, the loop filter) and Q20 (2SK19, PLL controlled VCO).
The difference between the frequency generated by the PLL (16.20 - 19.20 MHz) and the baseband frequency is then (through the ceramic filters) applied to the actual quadrature detector, U1 (3189). This detector demodulates the baseband audio signal.
The volume level is controlled by an analog voltage, applied to the "volume up/down" input. Q27 and Q28 select the required de-emphasis, as is given by table 2. Q23 acts as a buffer-stage and feeds into the audio line output and the RF modulator audio input.

Q27	Q28	mode
0	0	50 µsec
1	0	75 µsec
0	1	J17

(Logic level "1" means "switched on")

Table 2: De-emphasis select

Table 3 gives the relationship between audio subcarrier frequency and tuning voltage (PLL circuit). Diagram 5 represents the audio processing circuits.

Table 3: Audio subcarrier frequency versus tuning voltage.

Freq1	Freq2	Tv
5.50	16.20	3.22
6.20	16.90	4.14
6.50	17.20	4.57
6.60	17.30	4.72
6.65	17.35	4.80
6.80	17.50	5.03
7.02	17.72	5.37
7.20	17.90	5.65
7.38	18.08	5.94
7.56	18.26	6.23
7.62	18.32	6.32
8.00	18.70	6.94
8.20	18.90	7.27
8.50	19.20	7.77

Freq1 = displayed audio frequency
Freq2 = VCO frequency (Drain Q20)
Tv = tuning voltage (Pin 7, U8)

Frequencies given in MHz
Voltages given in VDC

(tolerance 2%)

5. RF-modulator

The modulator used to generate an UHF signal is a standard ALPS module. This signal can be adjusted on any channel in the range of (UHF) channel 30-40.

Two sound carrier standards are supported: PAL B/G (continental Europe) and PAL I (UK). A built-in switch selects the required sound format. It also has a built-in two stage line amplifier (20, 21) that can be used for the normal cable or terrestrial TV signals.

IC1 is the complex audio / video combiner and it even has an integrated four-bars test pattern generator.
The composite video signal is fed into the UHF oscillator, composed around Q5. VR1 adjusts the oscillator frequency.

Diagram 6 represents the UHF RF-modulator.

6. Microprocessor controller

The beating heart of the receiver is the Intel microprocessor 8085. This processor has an 8 bit databus and a 16 bits addressbus (64kbytes of memory are addressable).

U13 (LS373) is a standard address/data demultiplexer, required for proper operation (a 8085 has its databus multiplexed with the 8 least significant address bits).
U10 (LS155) is the address decoder ("memory mapper") that generates enabling signals (IO select) for the various memory chips and/or IO-devices.

There are 5 components in the memory map:

I. U11 (27128)
This Eprom contains the 8085 machine coded microprogram; this program controls all the actions, undertaken by the 8085.
It also contains satellite default tables, that is preset information regarding frequency, audio, bandwidth, etc.

II. U12 (28C16 or DS1220)
This EEprom (or non-volatile SRam) is used to store user preferences (for the satellite default tables).

III. U16 (8155)
The 8155 is a multi-functional IO chip. It converts all "one- line commands" issued by the frontpanel or the handheld into an 8-bit data format. It also generates control pulses for the actuator (positioner) circuit.
Furthermore, this chip handles all frequency related functions, like AFC and scanning.
U18 (LM348, opamp2) and U17 (555) form a serial A/D convertor. A "drifting" RF signal will be detected and compensated for.

IV. U14 (HC374) is used as a discrete D/A convertor. R141- 152 are an R-2R ladder-network, that does the actual conversion. U18 (LM348, opamp4) is a unity gain buffer, passing on an analog signal to the polarotor circuit, or in other words, control the skew.

V. U15 (HC374) is, like U14 is, a D/A convertor. The ladder network based around R157-169. U18 (LM348, opamp1) is the unity gain amplifier.
The analog signal controls the audio (volume) level.

The circuit around Q31 and Q32 generate a power-up reset pulse, forcing the microprocessor to execute a defined reset.

Diagram 7 represents the complete microprocessor circuits.

7. Front panel controller

The front panel controller translates pressing a button into a digital format, through which it can address U16 (8155) or U9 (8085) directly.

The front panel buttons are wired-up in a key-matrix to the main component, U701 (8279). U702 (HC138) acts as a multiplexer, required to form the matrix.
The output of U701 drives a display through a digital buffer, U703 (LS244).

The matrix also controls the common anode 3-digit display (this display gives information about video-frequencies, audio-frequencies, etc.) and 17 LED indicators (these LED's indicate features like bandwidth, de-emphasis, etc.).

Q701 and Q702 switch on and off the display, depending upon the power being switched on or off.
Q704 and U705 (LB1411) drive a 7-stage LED bar, indicating the relative field strength, proportional to the AGC signal coming from the demodulator.

An fully integrated InfraRed receiver translates commands from the Remote Control (handheld) into serial data. U16 (8155) converts these into the appropriate parallel digital format.

Diagram 8 represents the diagram of the front panel controller

The Remote Control is an extension of the front panel. It offers (nearly) all functions the front-panel does.
All functions are being taken care of by just one IC: U2001 (6122, an SMD device). It has a key-matrix and converts pressing a button into serial-data. This data controls 2001 (2SC710S), which drives a InfraRed LED.
The IC requires a ceramic resonator (Y2001, 455 kHz) to operate correctly.

Diagram 8a represents the diagram of the Remote Control.

8. Polarotor circuit

The polarotor circuit is a pulse width modulator, that can control stepping motors. It is controlled by an analog voltage.
U17 (555) is the complete pulse width modulator.
VR4 adjusts the correct offset (either horizontal or vertical). The so-called "Skew control in" is the analog control voltage.

Diagram 9 represents the polarotor circuit.

9. Actuator (positioner) circuit

This circuit requires some power to control the actuator and therefore it is fed from a separate transformer (T401).
Pressing "East" or "West" (on frontpanel or handheld) will be translated (by U16, the 8155) into a positive edged pulse, that will drive either the "East" or "West" circuit.

The "East" circuit consists of 401 and 402. Pressing the "East" button will cause 402 to switch relay KA, by which a voltage is applied to the positioner's motor.
The "West" circuit consists of 403 and 404. Pressing "West" will cause 404 to switch relay KB, which will apply a reversed voltage to the positioner. This will move the positioner in the opposite direction.

Feedback pulses, generated by an electro-magnetic switch that detects if the positioner is still moving, instruct the microprocessor circuits to continue or to stop sending power to the positioner.
These pulses are galvanically isolated by an opto-coupler (U401), before they are processed by the microprocessor IO- chip U16 (8155).

Diagram 10 represents the actuator circuit.

10. Power supply

The power supply generates 4 voltages:
*) +5 VDC (2A max)
*) +12 VDC (1A max)
*) +18 VDC (1A max)
*) +30 VDC (.5 A max)

To get reliable, stable voltages, the well-known 78-series linear power regulators are used.
U6 (3052, a power 7805) generates the +5 VDC.
U5 (7812) generates +12 VDC, for both internal and external circuits.
U4 (7818) generates +18 VDC, being used to power the LNB (external) circuits.
U3 (78L18) is used to generate +30 VDC, for which it also uses +12 VDC (from U5).
The main voltage (220-240 VAC) is transformed into lower voltages by a transformer. All power coming from this transformer is then single-end rectified (although symmetrical) by a diode-pair.
Diodes CR19, 24 generate a 21 VDC (with AC ripple). Diodes CR20, 23 generate +15 VDC; CR21, 22 generate 8 VDC.
For generating the +30 VDC, a voltage-doubler consisting of CR16, 17 and C87, 88 is used: this results in a +48 VDC on the input terminal of U3. The ripple-free +12 VDC is then fed into the "common" pin of U3, which results in the +30 VDC.

Q25 and Q26 are normally switched off (this means a low logic level for "Power cont in"), so that U6 gets the required DC to generate the +5V.
Even when the receiver is switched off (stand-by), the LNB is continuously being powered, as are the microprocessor circuits.

Diagram 11 represents the power supply.

11. MAC-preamplifier

This 3-stage transistor circuit provides the MAC output with an unclamped, unfiltered and de-emphasized video signal, able to drive MAC-decoders.

Q1 is a unity gain inverting amplifier. Q2 and Q3 are emitter-followers, used to get a matching output impedance.
The amplitude of the video signal should be slightly higher than 1.1 Vpp.

Diagram 12 represents the MAC-preamplifier.

SR-4500 : TROUBLE SHOOTING LIST

This list does not pretend to be an in-depth analysis as to how one should repair an SR-4500; it merely offers guidelines how to identify and solve (standard) problems.

Basically, there are 5 different problem levels:

1) Operational & control
2) Actuator/polarotor circuit
3) Video circuits
4) Audio circuits
5) RF circuits

1) OPERATIONAL & CONTROL

Receiver can not be switched on (stand-by indicator is lit)

- Check all powerlines for the presence of the correct voltage levels.
- Check pin 15 of U10 (8155). The logic level should be "1" when switched on and "0" when switched off (stand-by).
- Check Q25 and Q26.
- Check K1.
- Check for presence of main clock signal on pin 2 and 3 of U9(8085).
- Check front panel circuit board:
  Data streams should be seen on pins 24-31 of U701 (8279), as well as on pins 32-34.
  The frontpanel buttons are organised as 6*3 matrix: check U701 (8279) and U702 (74HC138) for correct performance.

Three digit display displays garbage

- Check output-pins of U703 (74LS244) for multiplexed display signals.
- Check Q705-709 (KN2907) for correct enabling the display.

Receiver locks-up: several indicators are lit, but normal operation is not possible

- Carry out the 80085-modification.
- Check U11 (Eprom 27128, should be dated 03/21/88).
- Check U12 (Eprom DS1220 or 28C16).

Remote control unit doesn't work

- Check pins 10 and 11 of Q2001 (6122) for a 455 kHz signal.
- Check for pulse width modulated signal at pin 7 of U2001 (6122).
- Check Q2001 (2SC2710) and CR2001 (EL-IL2) for being open-circuit.
- Check SG-05 (Infra-red sensor).

Remote control LED indicator lights intermittently

- Replace red plastic filter.
- Check SG-05 (Infra-red sensor).

2) ACTUATOR / POLAROTOR CIRCUITS

Polarotor can not make a full 90 degrees turn

- Check U7 (555) for pulse width modulated signal on pin 3, when pressing the skew buttons.
- Adjust VR1.
- Check U13 (should be a 74HC374).

Polarotor doesn't work

- Check U7 (555) for pulse width modulated signal on pin 3, when pressing one of the skew buttons.
- Check the presence of an input-signal at R187 and pin 5 of U7 (555), when pressing one of the skew buttons.
- Check R125 and 126 for correct values.

Actuator can't be moved: ER3 shown on display

- Check reed switch in actuator.
- Check presence of actuator feedback pulse at pin 2 of U401 (4N26). The same pulse (galvanically isolated) should be present at pin 5 of U401 (4N26).
- Check Q33 (2SA652) and CR32 (1N4148) for shortcircuiting.

No West movement

- Check pin 36 of U16 (8155) for change of logic level, when West key is pressed. Check Q401 (2SC1959), Q402 (BC300) and CR404 (1N4004) for shortcircuiting.

No East movement

- Check pin 35 of U16 (8155) for change of logic level, when East key is pressed. Check Q403 (2SC1959), Q404 (BC300) and CR406 (1N4004) for shortcircuiting.

3) VIDEO CIRCUITS

Clamp doesn't work

- Check pin 21 of U16 (8155) for change of logic level when pressing Clamp button.
- Check C26.
- Check Q17 (2SC174) and relay K3.

Video polarity can not be changed

- Check pin 34 of U16 (8155) for change of logic level when pressing Polarity button.
- Check Q5 (2SC1740)

No baseband video output

- Check Q8 (2SC1740) for shortcircuiting.
- Check C15 and L4.

4) AUDIO CIRCUITS

No audio

- Check Q23 (2SC1740).
- Check R94-96 and C61.
- Check outputs (pins 1,2,4,5) of U19 (4052) for change of logic level when changing bandwidth.

Distorted audio

- Check U1 (3189) pin 1 for baseband signal and pin 6 for demodulated signal.
- Adjust VC1.

Audio tuning not possible

- Check Connector P102, pin 2 for presence of baseband signal.
- Check output of BP-70E band pass filter for presence of filtered baseband signal.
- Check audio PLL loop, built around U2 (MC145155).
  When tuning, a changing waveform should be visible at pin 6 (Phase Detector output). A changing DC voltage should be measured at pin 7 of U18 (LM358). The DC voltage is proportional to the frequency, ie. a higher frequency is related to a higher voltage.
- Check drain of Q20 (2SK19) for changing frequency.
- Check output of mixer Q19 (3SK74) for changing frequency.

5) RF CIRCUITS

Receiver will not tune properly onto a channel

- Check RF PLL loop, built around U201 (MC145155).
  When tuning a changing waveform should be visible at pin 6 (Phase Detector output). A changing DC voltage should be measured at pin 1 of U202 (LM358). The DC voltage is proportional to the frequency, ie. a higher frequency is related to a higher voltage.

No picture; signal strength meter doesn't work; standby indicator doesn't work

- Check fuse F101 (a .5 Amp fuse) for being open-circuit.
- Check pin 3 of U4 (7818) for correct output voltage, which is 18 VDC.

No picture; signal strength meter doesn't work; standby indicator is lit

- Check all pins of connector P102 for presence of signals.

No RF modulator UHF signal

- Check for presence of 12 VDC.
- Check Q16 and R58, 59.

AFC doesn't work

- Check connector P102, pin 2 for the presence of baseband signal, as well as U18 (LM324), pin 14.
  A pulse width modulated signal should be present at U17 (555), pin 3 (TP2).

SR-4500 : IC PIN OUTS

The following Integrated Circuits are used in the SR-4500.

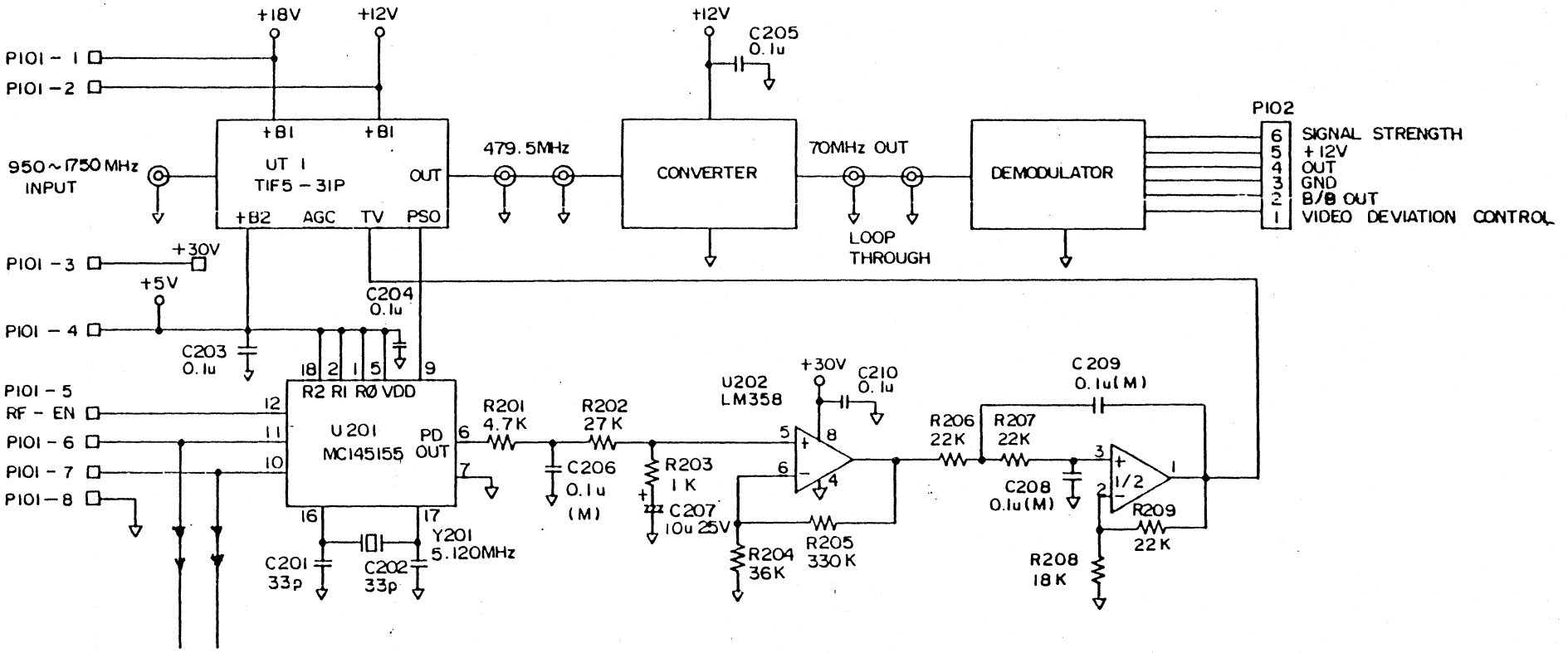
Name	Family Name	Function
U1	CA 3189	FM IF Subsystem
U2	MC 145155	Serial input PLL frequency synthesizer
U3	7818	Fixed output positive voltage regulator
U4	78L18	Fixed output positive voltage regulator
U5	7812	Fixed output positive voltage regulator
U6	ST3052	Fixed output positive voltage regulator
U7	NE 555	General purpose timer circuit
U8	LM 358	Dual operational amplifier
U9	8085	8bit HMOS microprocessor
U10	74LS155	Dual 2-to-4 line decoder
U11	27(C)128	16k * 8 bits Eprom
U12	28C16(DS1220)	(Pseudo) Eprom
U13	74LS373	Octal D-latch (low power Schottky)
U14	74HC374	Octal D-flip-flop (high speed CMOS)
U15	74HC374	Octal D-flip-flop (high speed CMOS)
U16	8155	2k * 8 bits SRam / timer / IO ports
U17	NE 555	General purpose timer circuit
U18	LM 324	Quad operational amplifier
U19	4052	Dual 4-channel analog multiplexer
U101	78L05	Fixed output positive voltage regulator
U102	78L05	Fixed output positive voltage regulator
U103	MC 10216	Three stage voltage controlledamp
U104	MC 1496P	Double balanced demodulator
U201	MC 145155	Serial input PLL frequency synthesizer
U202	LM 358	Dual operational amplifier
U401	4N26	Opto-coupler
U701	8279	Keyboard / display interface
U702	74HC138	3-to-8 line decoder (high speed CMOS)
U703	74LS244	Octal buffer (low power Schottky)
U705	LB 1411	Flash convertor
U2001	6122	One chip remote control circuit

The following transistors are used in the SR-4500 :

Name	Family	Parameters	Pinout
(70 MHz convertor board)			
Q1	2SC2734	NPN, 20V / 50 mA	P1
Q2	2SC3356	NPN, 20V / 100 mA	P2
Q3	2SC2735	NPN, 30V / 50 mA	P3
(AV-board)			
Q1	2SC1740	NPN, 50V / 100 mA	P4
Q2	2SC1740	NPN, 50V / 100 mA	P4
Q3	2SC1740	NPN, 50V / 100 mA	P4
Q4	2SC1740	NPN, 50V / 100 mA	P4
Q5	2SC1740	NPN, 50V / 100 mA	P4
Q6	2SC1740	NPN, 50V / 100 mA	P4
Q7	2SC1740	NPN, 50V / 100 mA	P4
Q8	2SC1740	NPN, 50V / 100 mA	P4
Q9	2SC1740	NPN, 50V / 100 mA	P4
Q10	2SC1740	NPN, 50V / 100 mA	P4
Q11	2SC1740	NPN, 50V / 100 mA	P4
Q12	2SC1740	NPN, 50V / 100 mA	P4
Q13	2SC1740	NPN, 50V / 100 mA	P4
Q14	2SC1740	NPN, 50V / 100 mA	P4

The following transistors are used in the SR-4500 :

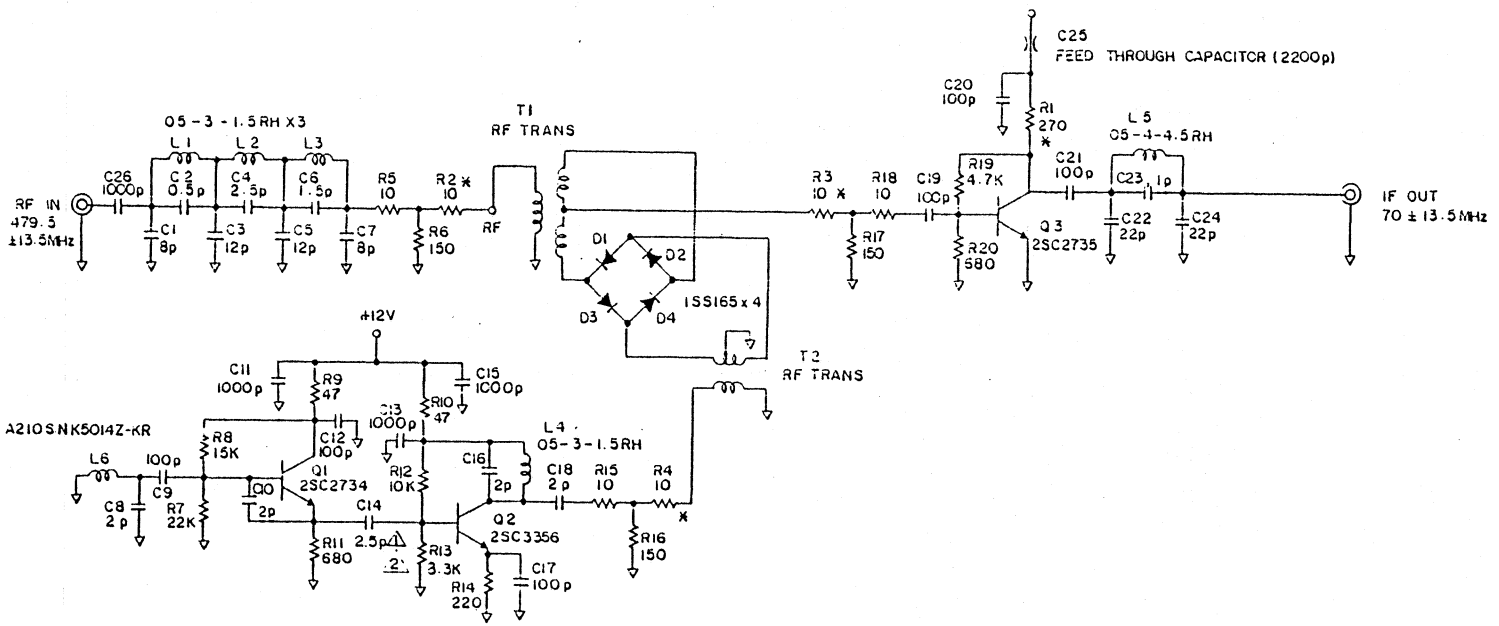
Name	Family	Parameters	Pinout
(AV-board, continued)			
Q15	2SC1740	NPN, 50V / 100 mA	P4
Q16	2SC1740	NPN, 50V / 100 mA	P4
Q17	2SC1740	NPN, 50V / 100 mA	P4
Q18	2SC1740	NPN, 50V / 100 mA	P4
Q19	3SK74	Dual gate MOS-Fet	P5
Q20	2SK19	N-ch FET/18V/25 mA	P6
Q22	2SC1959	NPN, 35V / 500 mA	P4
Q23	2SC1740	NPN, 50V / 100 mA	P4
Q24	2SC1959	NPN, 35V / 500 mA	P4
Q25	2SA562	PNP, 30V / 300 mA	P4
Q26	BC300	NPN, 120V / 1 A	P7
Q27	2SC1740	NPN, 50V / 100 mA	P4
Q28	2SC1740	NPN, 50V / 100 mA	P4
Q31	2SC1959	NPN, 35V / 500 mA	P4
Q32	2SC1959	NPN, 35V / 500 mA	P4
Q33	2SA562	PNP, 30V / 300 mA	P4
(Demodulator board)			
Q102	2SC2734	NPN, 20V / 50 mA	P1
Q103	2SC2734	NPN, 20V / 50 mA	P1
Q104	2SC1740	NPN, 50V / 100 mA	P4
Q105	2SC1740	NPN, 50V / 100 mA	P4
Q106	2SC1740	NPN, 50V / 100 mA	P4
Q107	2SC2734	NPN, 20V / 50 mA	P1
Q108	2SC2734	NPN, 20V / 50 mA	P1
Q109	2SC2734	NPN, 20V / 50 mA	P1
Q110	2SC2412	NPN, 50V / 100 mA	P4
Q111	2SA562	NPN, 30V / 300 mA	P4
Q112	2SC1740	NPN, 50V / 100 mA	P4
Q113	2SC1740	NPN, 50V / 100 mA	P4
(Actuator board)			
Q401	2SC1959	NPN, 35V / 500 mA	P4
Q402	BC300	NPN, 120V / 1 A	P7
Q403	BC300	NPN, 120V / 1 A	P7
Q404	2SC1959	NPN, 35V / 500 mA	P4
(Front panel board)			
Q701	2SA562	PNP, 30V / 300 mA	P4
Q702	2SC1959	NPN, 35V / 500 mA	P4
Q704	2SA562	PNP, 30V / 300 mA	P4
Q705	KN2907	PNP, 60V / 600 mA	P3
Q706	KN2907	PNP, 60V / 600 mA	P3
Q707	KN2907	PNP, 60V / 600 mA	P3
Q708	KN2907	PNP, 60V / 600 mA	P3
Q709	KN2907	PNP, 60V / 600 mA	P3
(Remote control board)			
Q2001	2SC2710S	NPN, 35V / 800 mA	P8



ECHOSTAR

SR-4500

Diagram 1: Tuner



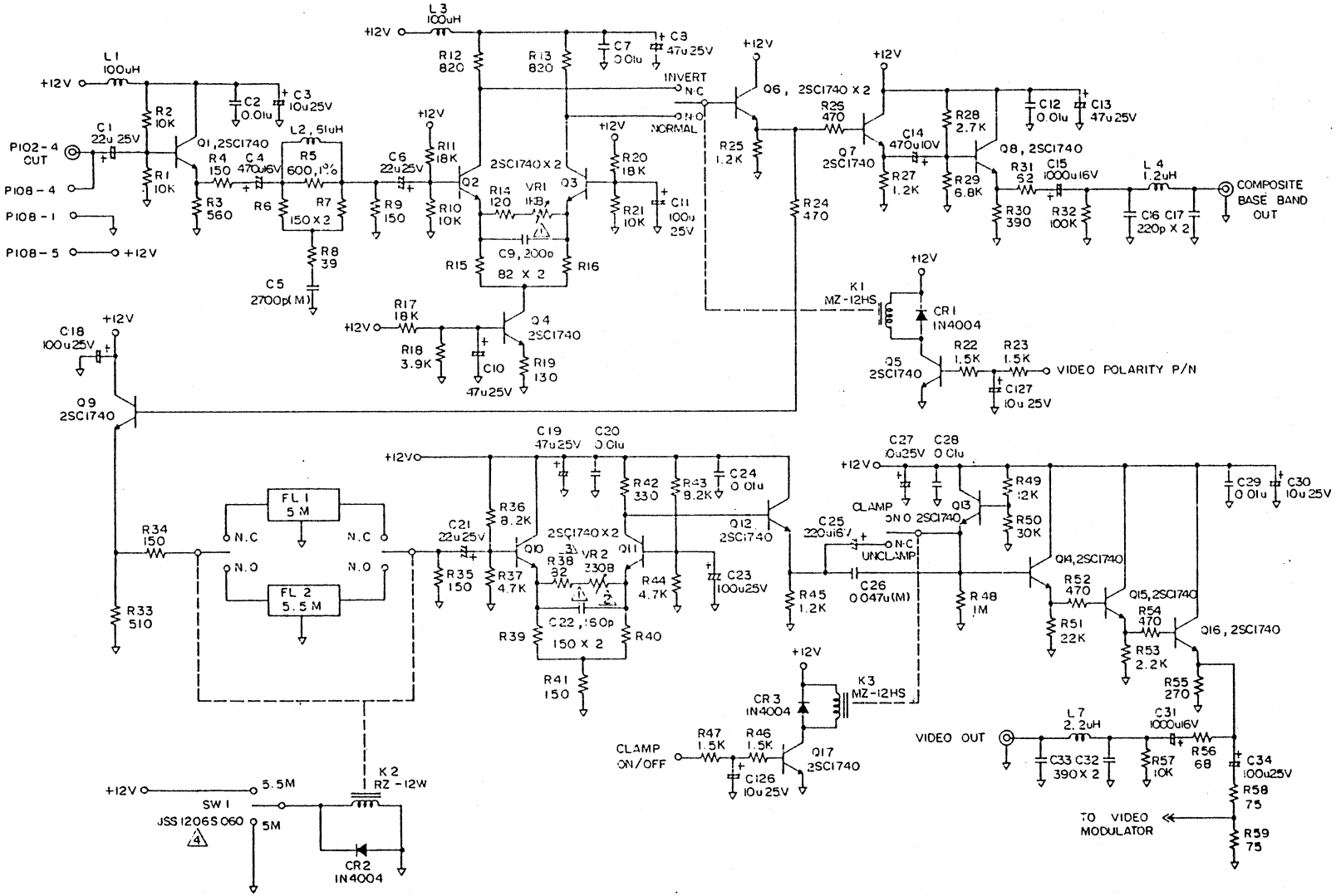
NOTE :

1. * : CARBON FILM RESISTOR (1/8W)
THE OTHER CHIP COMPONENT

ECHOSTAR

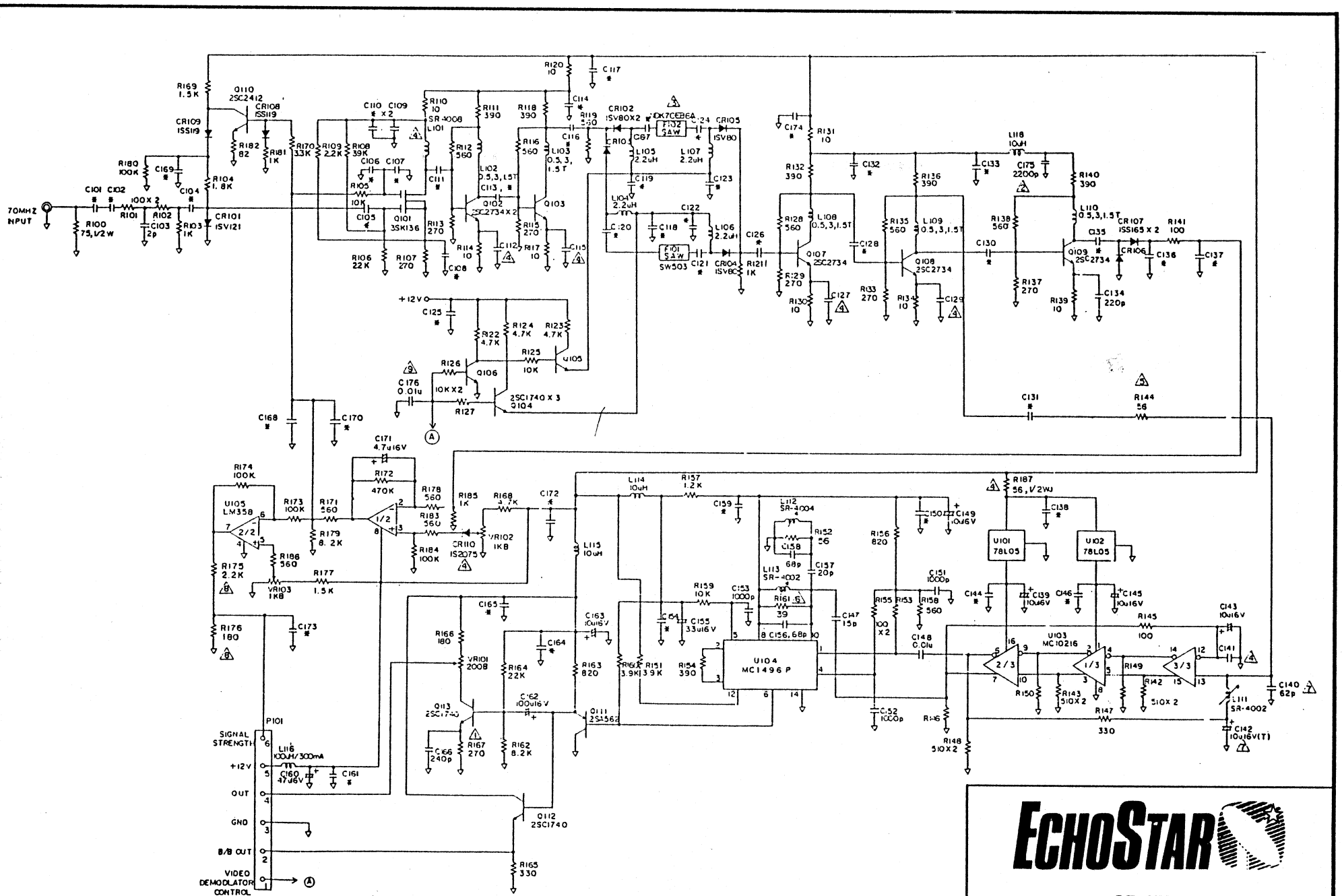
SR-4500

Diagram 2: Second Down-converter



SR-4500

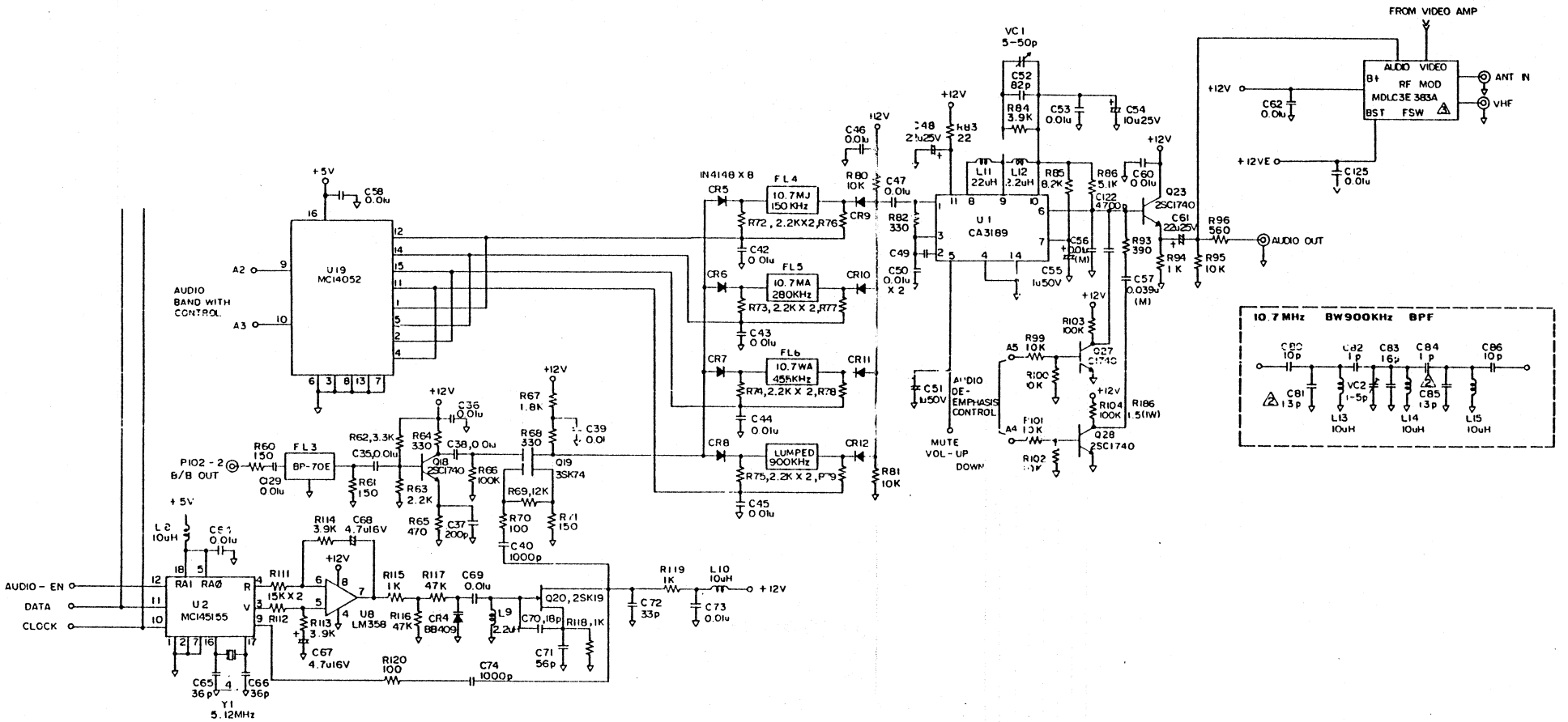
Diagram 4: Video Processing Circuits



ECHOSTAR

SR-4500

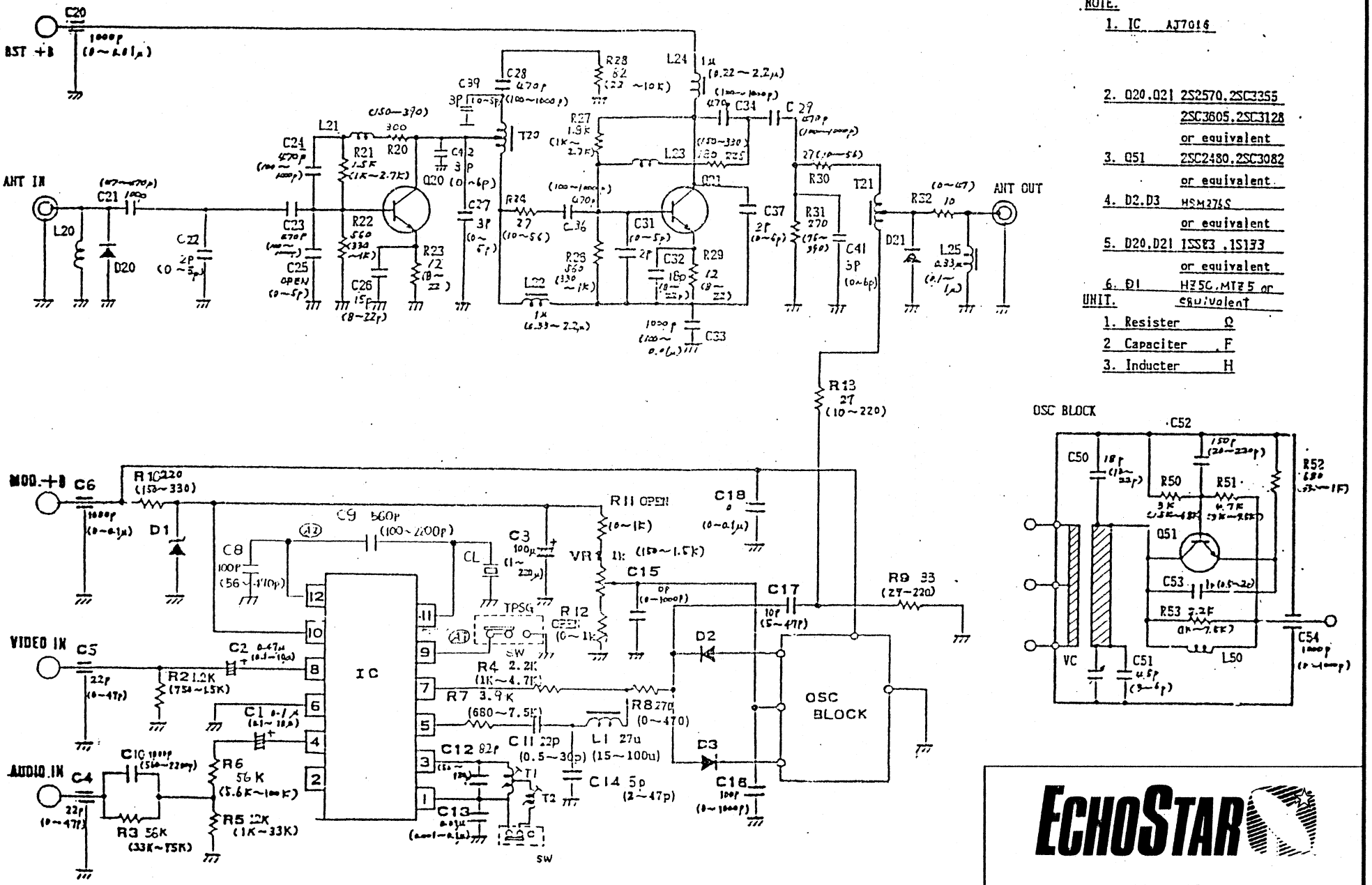
Diagram 3: Demodulator



ECHOSTAR

SR-4500

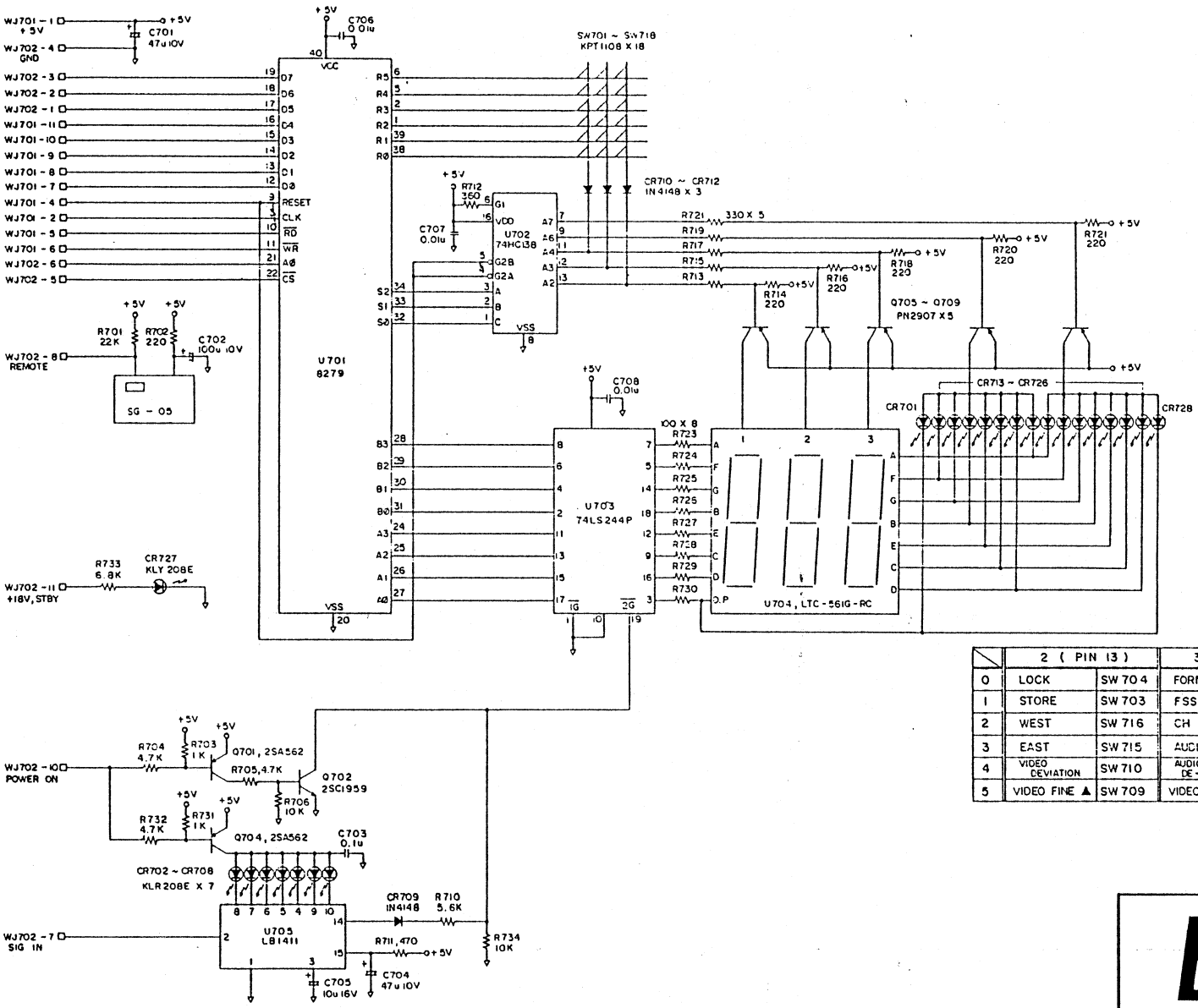
Diagram 5: Audio Processing



ECHOSTAR

SR-4500

Diagram 6: UHF RF-modulator



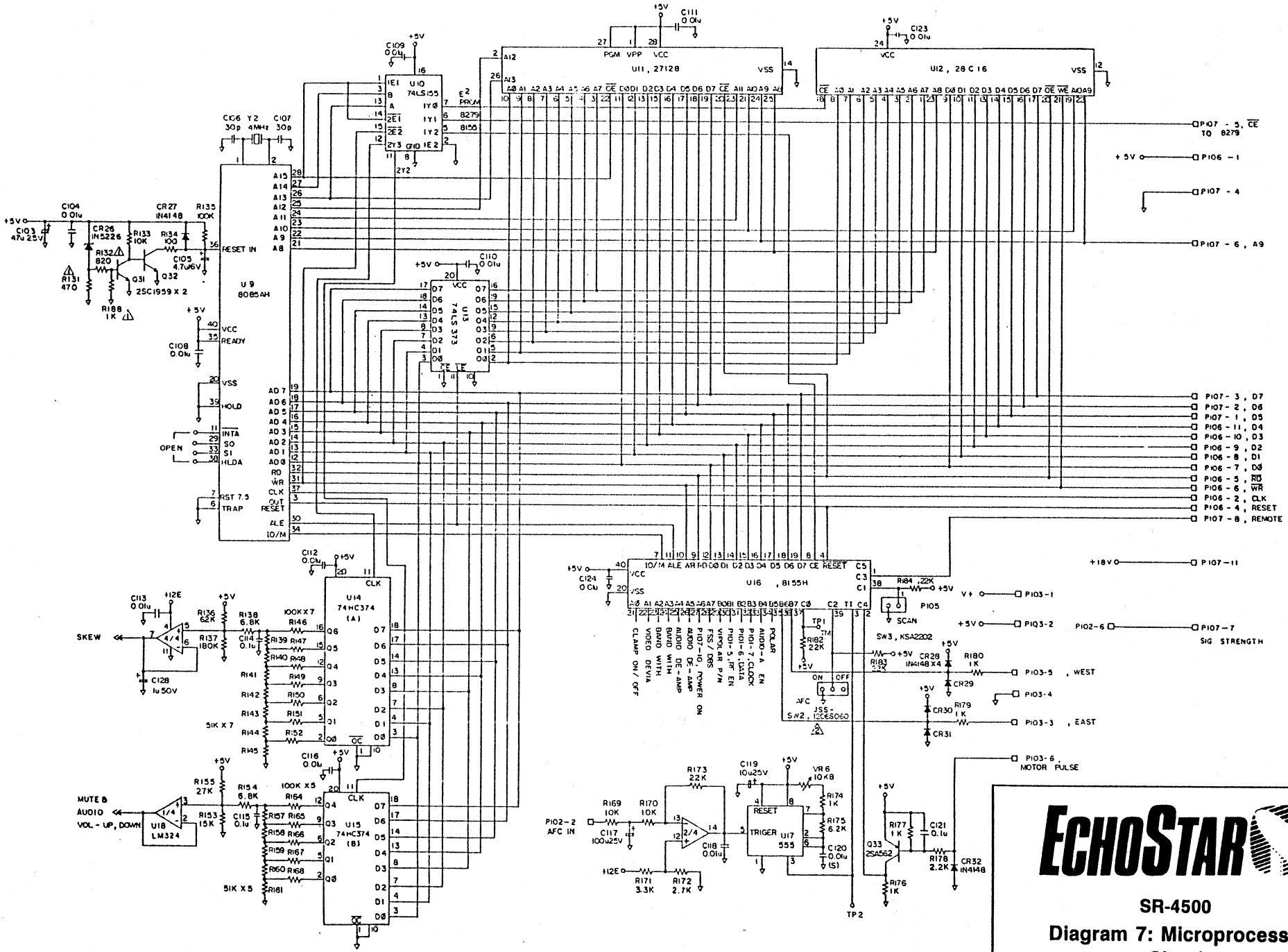
701	FSS / DBS	KLG - 208E
713	CLAMD	KLG - 208E
714	LOCK	KLG - 208E
715	POLAR P/N	KLG - 208E
716	REMOTE	KLG - 208E
717	J17	KLR - 208E
718	NARROW	KLG - 208E
719	50uS	KLR - 208E
720	VERT	KLG - 208E
721	HORIZ	KLG - 208E
722	130	KLG - 208E
723	ANT. POSITION	KLR - 208E
724	400	KLG - 208E
725	900	KLG - 208E
726	280	KLG - 208E
728	75uS	KLR - 208E

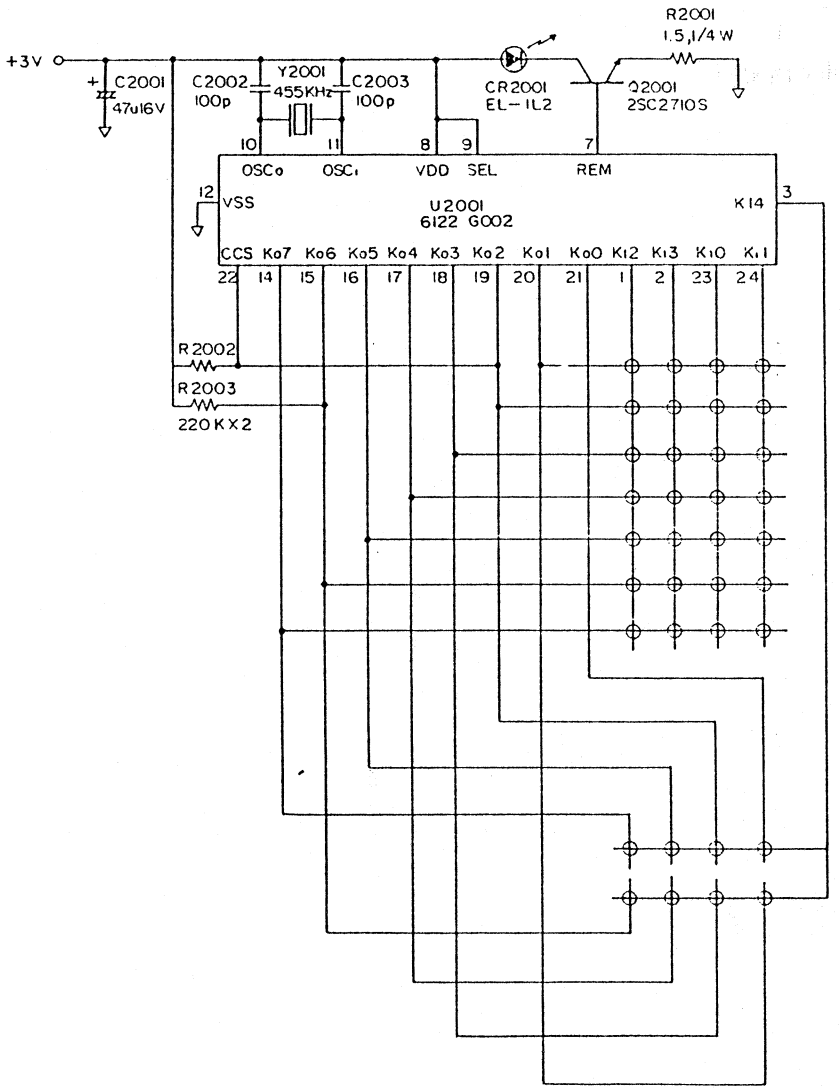
	2 (PIN 13)		3 (PIN 12)		4 (PIN 11)	
0	LOCK	SW 704	FORMAT	SW 705	SKEW ▼	SW 706
1	STORE	SW 703	FSS / DBS	SW 702	POWER	SW 701
2	WEST	SW 716	CH ▼	SW 717	CH ▲	SW 718
3	EAST	SW 715	AUDIO ▲	SW 714	AUDIO ▼	SW 713
4	VIDEO DEVIATION	SW 710	AUDIO DE-EMPHASIS	SW 711	BANDWIDTH	SW 712
5	VIDEO FINE ▲	SW 709	VIDEO FINE ▼	SW 708	SKEW ▲	SW 707

ECHOSTAR

SR-4500

Diagram 8a: Front Controller Panel


U9 8085AH
U10 74LS155
U11, 27128
U12, 28C16
U13 74LS373
U14 74HC374 (A)
U15 74HC374 (B)
U16, 8155H
U17 555
U18 LM324
RESET IN
RESET OUT
READY
HOLD
INTA
SO
SI
HLDA
RST 7.5
TRAP
ALE
IO/M
RD
WR
CLK
SKEW
MUTE & AUDIO VOL - UP, DOWN
AFC IN
SCAN
SW3, KSA2202
SW2, ISS-ISS6S060
TP1
TP2
P107 - 5, CE TO 8279
P106 - 1
P107 - 4
P107 - 6, A9
P107 - 3, D7
P107 - 2, D6
P107 - 1, D5
P106 - 11, D4
P106 - 10, D3
P106 - 9, D2
P106 - 8, D1
P106 - 7, D0
P106 - 5, RD
P106 - 6, WR
P106 - 2, CLK
P106 - 4, RESET
P107 - 8, REMOTE
+18V
P107 - 11
V+
P103 - 1
P103 - 2
P102 - 6
P107 - 7
SIG STRENGTH
P103 - 5, WEST
P103 - 4
P103 - 3, EAST
P103 - 6, MOTOR PULSE
P102 - 2
P105
ECHOSTAR
SR-4500
Diagram 7: Microprocessor Circuit



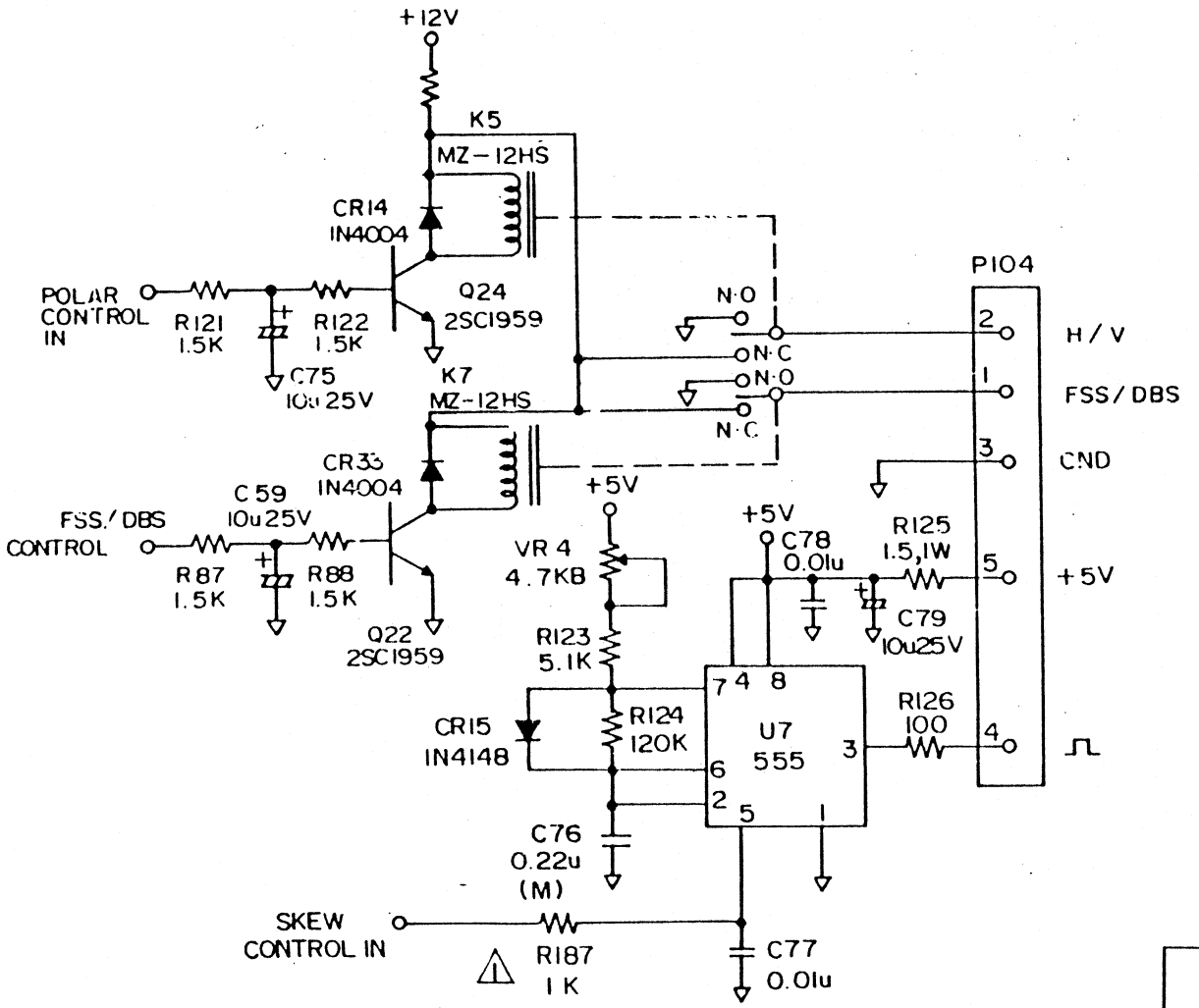
((CODE TABLE))

EAST	A0	SAT	20	WEST	E0	POWER	60
LOCK		POSITION		▼ SKEW		▼ SKEW	
1	90	2	10	3	D0	FORMAT	50
4	B0	5	30	6	F0	CH ▲	70
7	88	8	08	9	C8	CH ▼	48
ERASE	98	0	18	PRG	D8	FCH	58
VIDEO DEVIA	B8	MUTE	38	BANDWIDTH	F8	AUDIO DE-EMP	78
POLARITY	1A	CLAMP	22	▼ AUDIO	2A	▲ AUDIO	12
▼ VIDEO FINE	3A	▲ VIDEO FINE	32	▼ VOLUME	0A	▲ VOLUME	02

ECHOSTAR

SR-4500

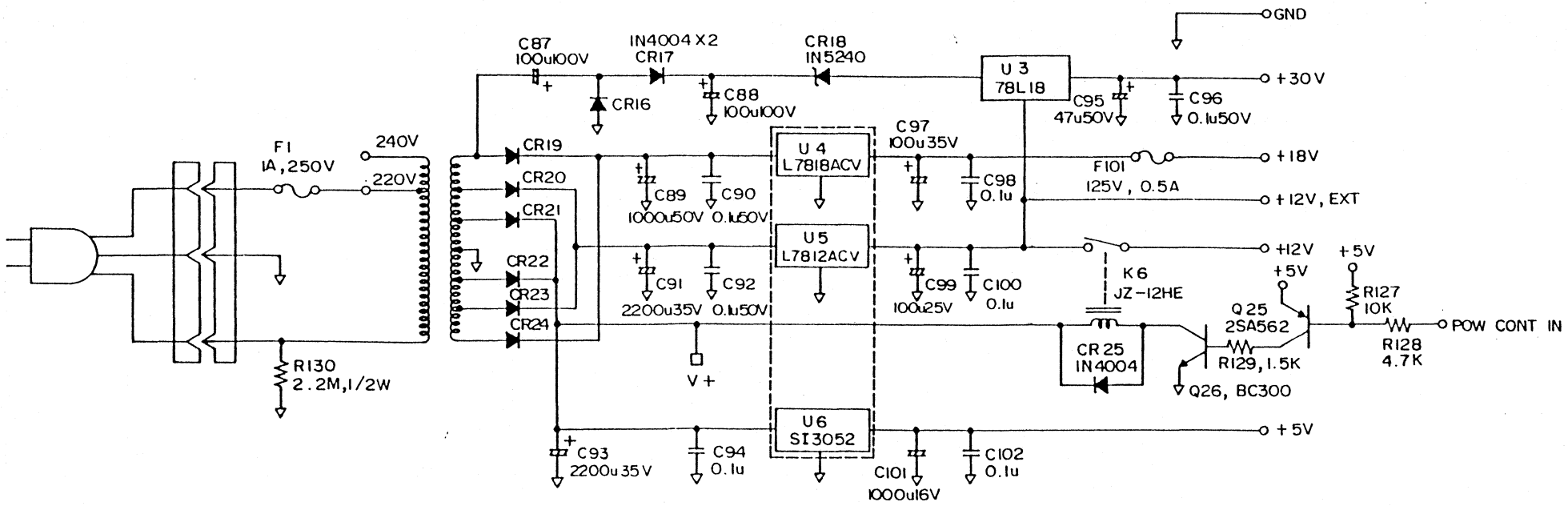
Diagram 8b: Remote Control (handheid)



ECHOSTAR

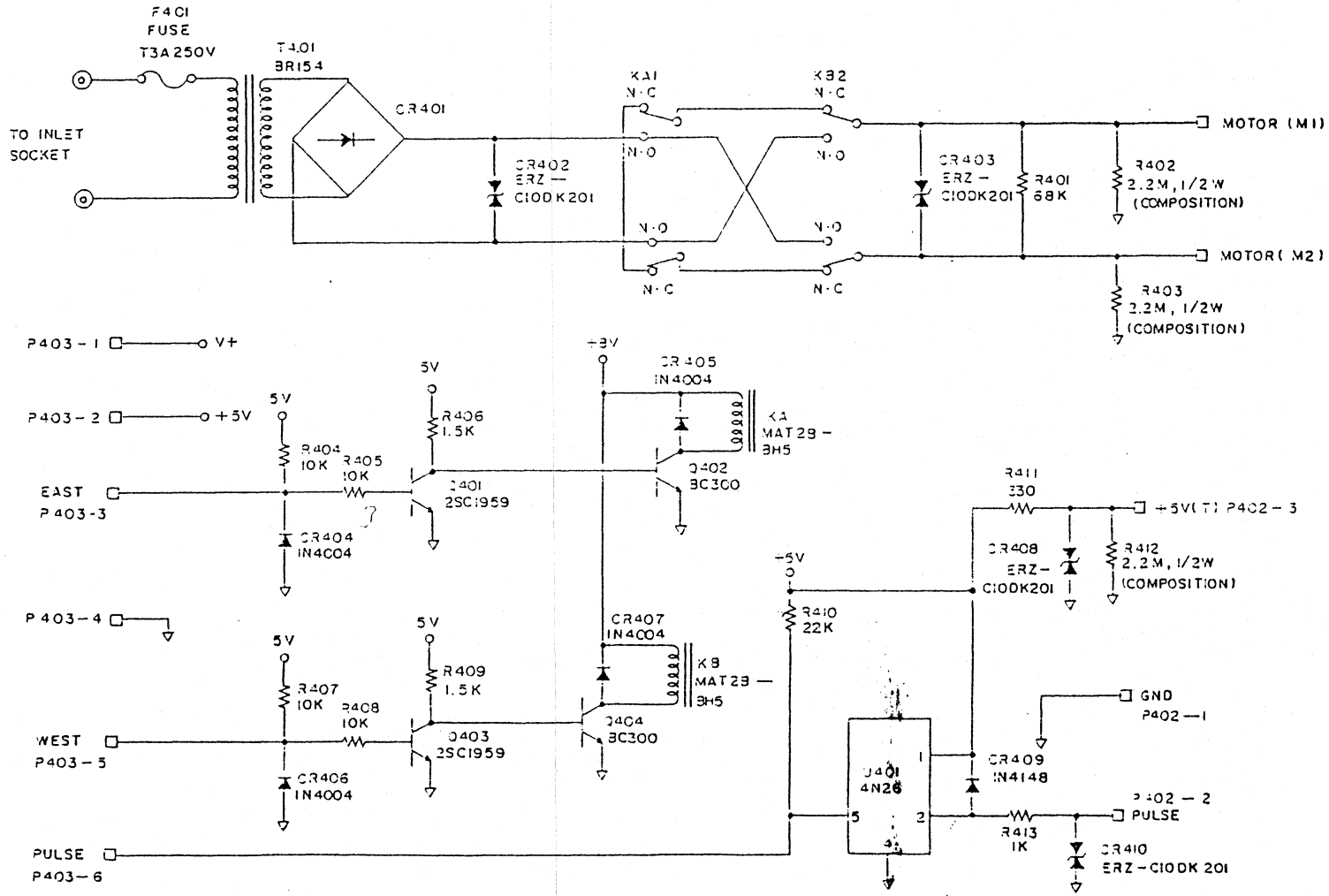
SR-4500

Diagram 9: Polarotor Circuit



SR-4500

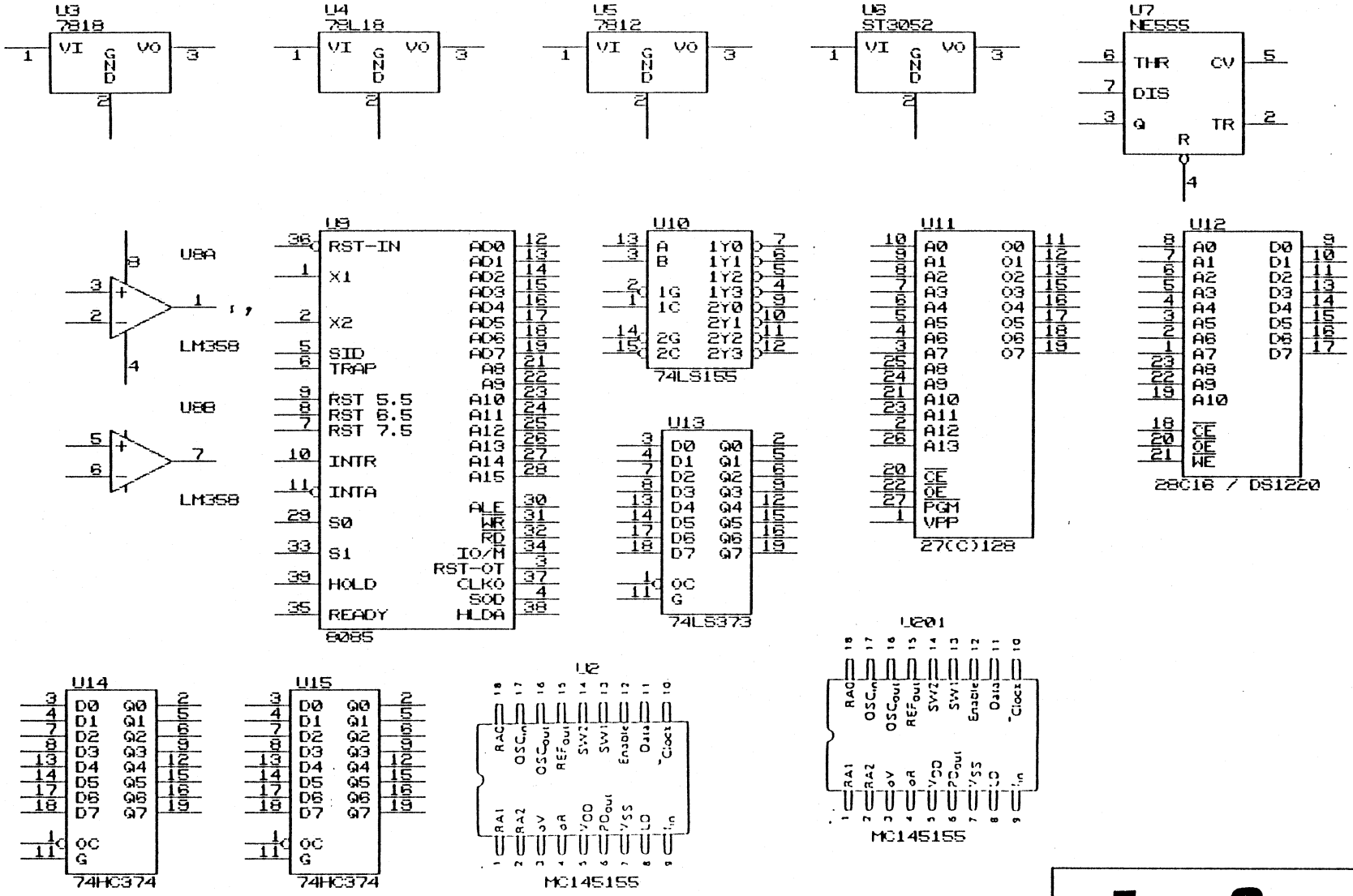
Diagram 11: Power Supply



ECHOSTAR

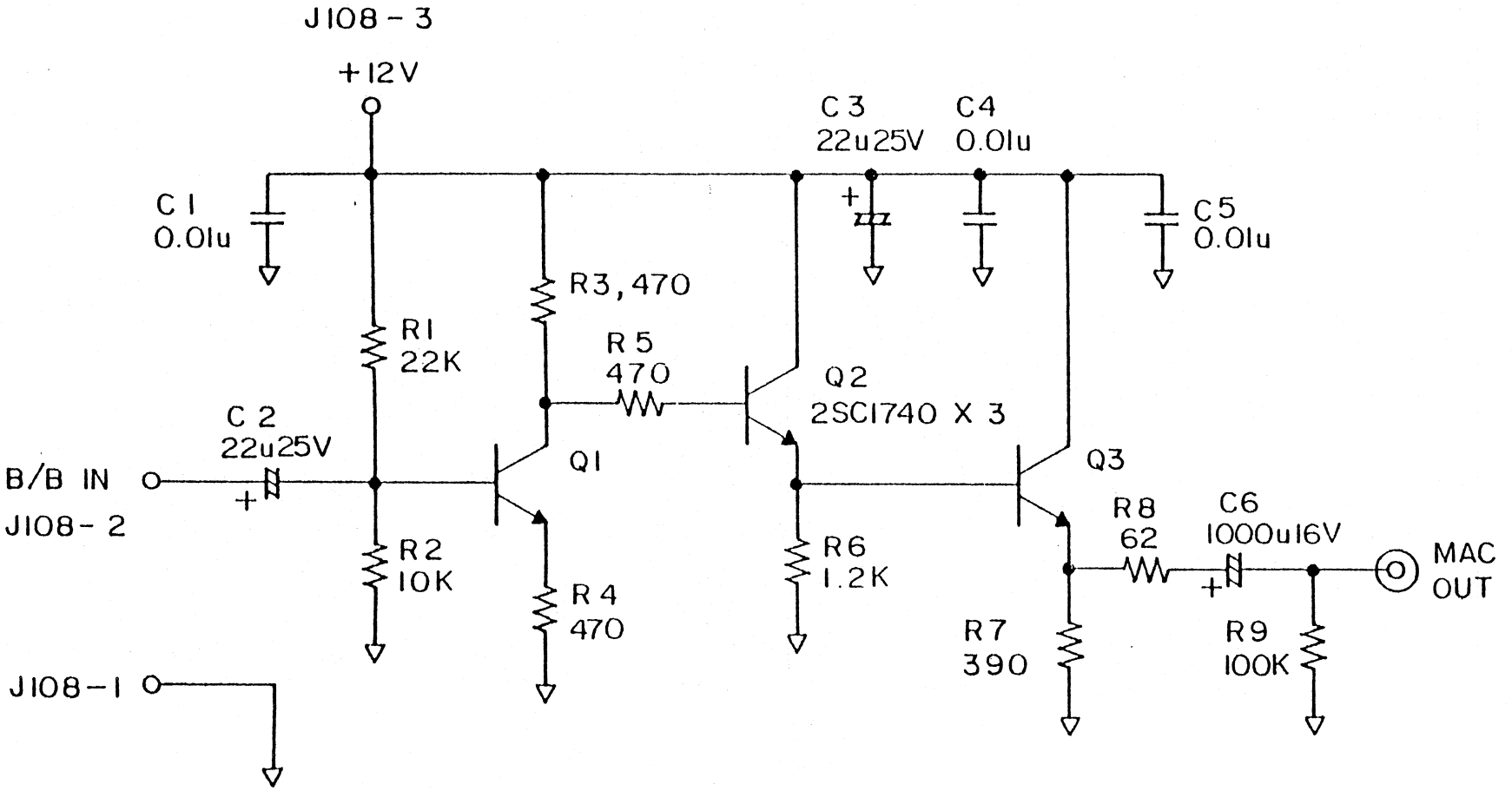
SR-4500

Diagram 10: Actuator (Positioner) Control Circuit



SR-4500

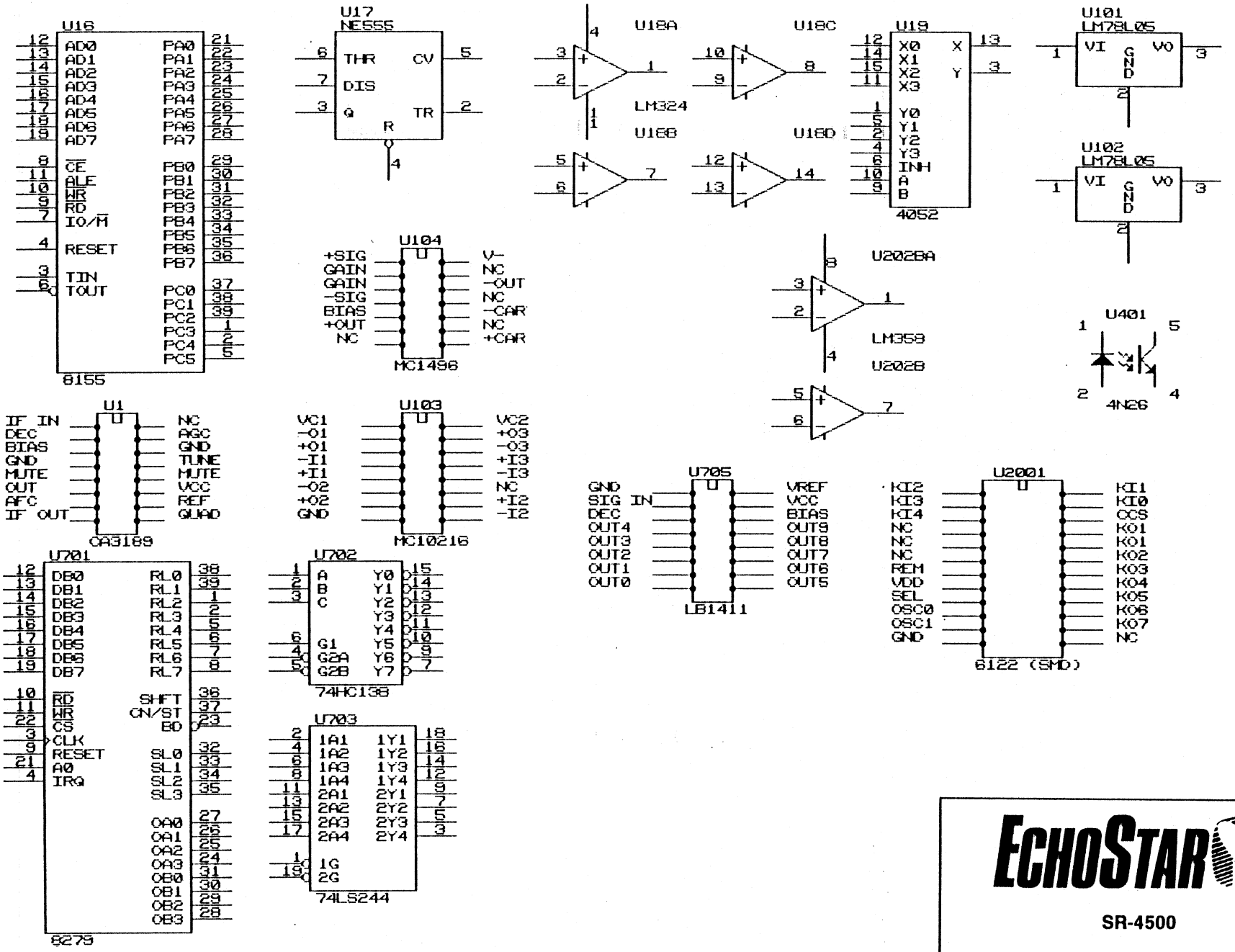
Diagram 13: IC pinouts 1



ECHOSTAR

SR-4500

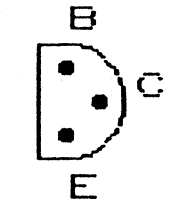
Diagram 12: MAC Preamplifier



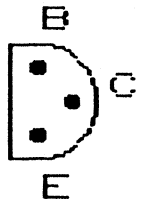
ECHOSTAR

SR-4500

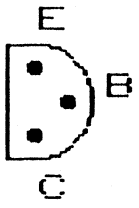
Diagram 14: IC pinouts 2



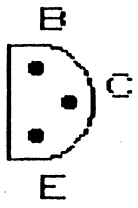
P1



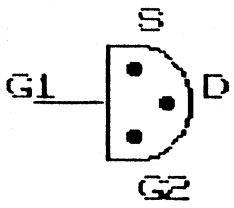
P2 (SMD)



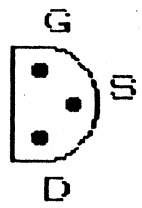
P3



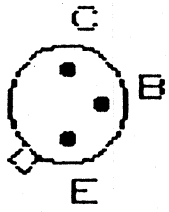
P4



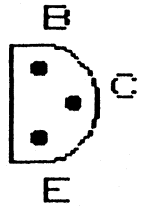
P5



P6



P7

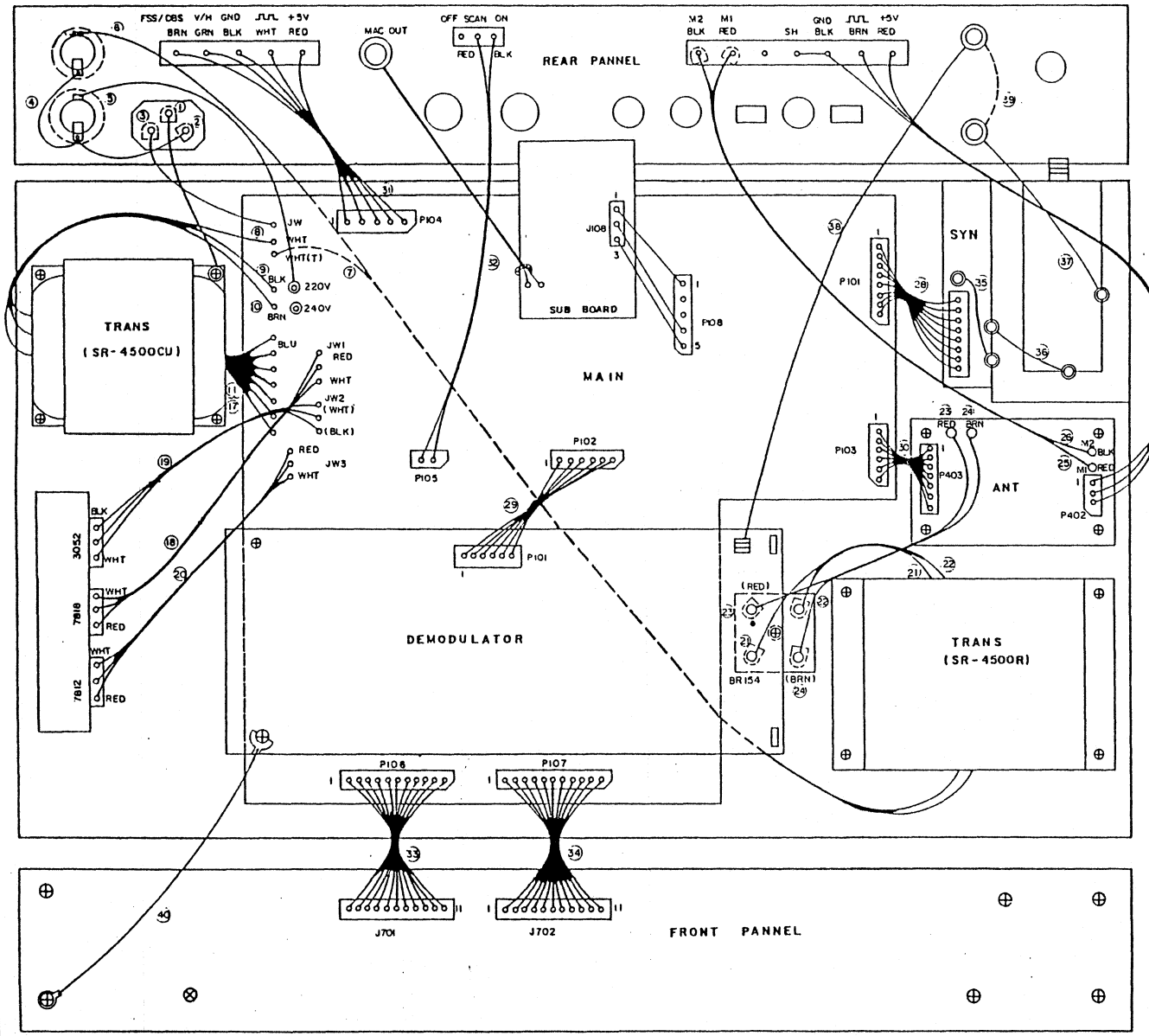


P8 (SMD)

ECHOSTAR

SR-4500

Diagram 15: Transistor pinouts



JUMPER WIRE (GND)		40	BLACK	110	1015 ¤ 22
COAXIAL CABLE		39	"	100	F 59 ASS'Y
COAXIAL CABLE		38	"	220	PHONE ASS'Y
	870022	37	"	160	RCA PHONE TO PHONE PLUG A'
	870021	36	"	120	"
	SW1472	35	"	110	PHONE ASS'Y
P107 (MAIN ↔ FRONT)		34	PIN1. YELLOW, 11p FLAT	190	1007 ¤ 26
P106 (MAIN ↔ FRONT)		33	PIN1. YELLOW, 11p FLAT	"	
P105 (MAIN ↔ REAR)		32	PIN1. RED, 2. BLACK	150	
P104 (MAIN ↔ TERMIAL)		31	PIN1. BRN, 2. GRN, 3. BLK 4. WHT 5 RED	125	
P103 (MAIN ↔ ANT)		30	PIN1. YELLOW, 6p FLAT	60	
P102 (MAIN ↔ DEMOD)		29	" , "	160	
P101 (MAIN ↔ SYN)		28	" , 8p "	"	
P402 (ANT ↔ TERMINAL)		27	PIN1. BLK, 2. BRN, 3 RED	280	1007 ¤ 26
JUMPER-WIRE (ANT ↔ TERMINAL)	JW11	26	BLACK 2p	270	1015 ¤ 22
		25	RED FLAT	"	
JUMPER-WIRE (ANT ↔ BR154)	JW10	24	BROWN	160	
	JW9	23	RED	"	
POWER TRANSFORMER (SR4500R-BR154)		22	"	150	
		21	"	"	1015 ¤ 22
3p CONN.ASS'Y (MAIN → I-C)	JW3	20	PIN1. RED, 2. BLK, 3 WHT	180	1007 ¤ 24
	JW2	19	PIN1. WHT, 3. RED, 5 BLK	"	
	JW1	18	PIN1. RED 2. BLK 3. WHT	190	1007 ¤ 24
POWER TRANSFORMER (SR-4500CU)		17	BLACK	140	1007 ¤ 22
		16	YELLOW		
		15	"		
		14	RED		
		13	"		
		12	BLUE		
		11	"	140	1007 ¤ 22
		10	BROWN	200	1015 ¤ 22
		9	BLACK	"	
		8	WHITE	"	
POWER TRANSFORMER (SR-4500R)		7	"	480	
		6	BLACK	570	
JUMPER-WIRE (POWER)	JW4	5	BROWN	170	
	JW8	4	"	90	
	JW5	3	BLUE	140	
	JW7	2	BROWN	130	
JUMPER WIRE (GND)	JW6	1	GREEN	70	1015 ¤ 22
CONNECTION		NO	COLOR	LENGTH (mm)	TRICK (AWG)

ECHOSTAR

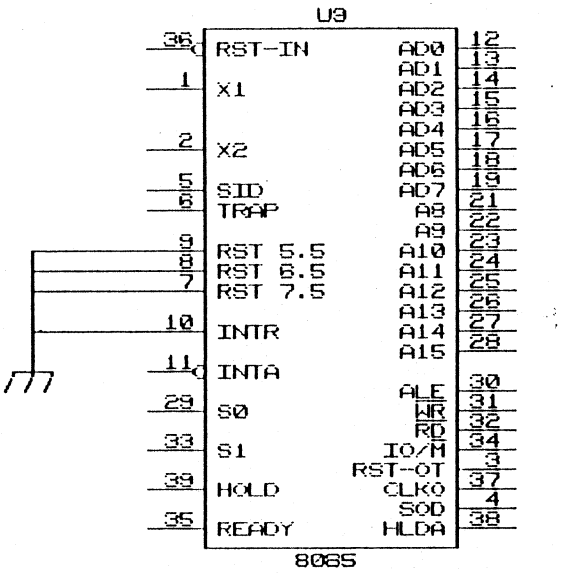
SR-4500

Diagram 17: Wire Diagram

This modification only applies to official Echostar distributors.

It should be carried out by a qualified technician, otherwise the warranty will be voided !

The modification should only be carried out on models manufactured before October 1988 (ie. serial number is lower than E8K).



This modification will cure the "lock-up" problems.

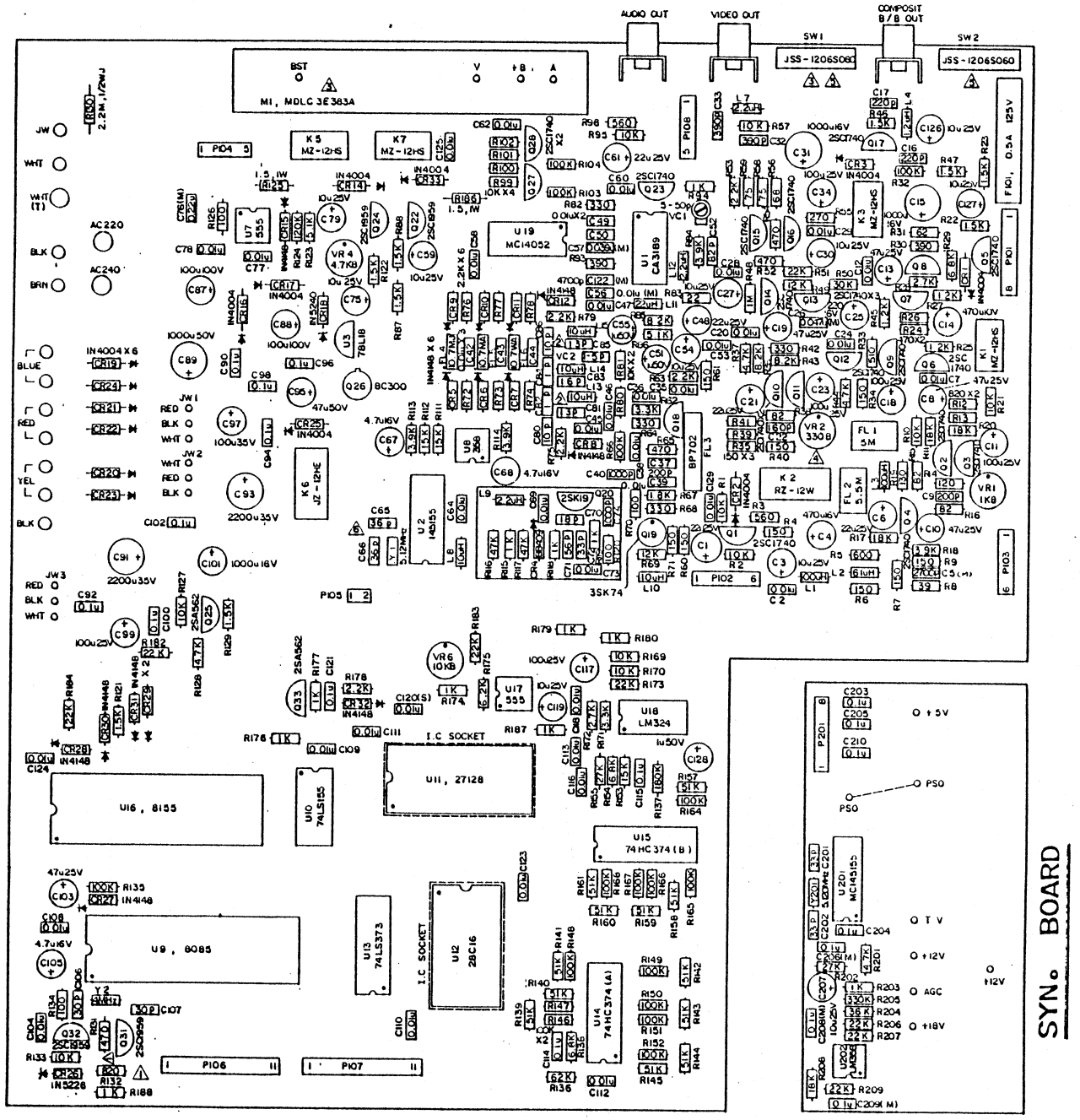
Locate U9 (8085 microprocessor) on the main circuit board.
Solder pins 8,9 and 10 to pin 7.
Effectively, you will "ground" the mentioned pins.
(Pin 7 is already connected to ground)

The modification will prevent the 8085 from getting (digital) noise signals on the indicated input-lines.
The noise will cause the 8085 to "lock-up".

ECHOSTAR

SR-4500

Diagram 16: 8085 Modification



1987. 5. 27	1	· R131(100→470), R132(100→820) · R188(1K) 삭제 97I.		
1987. 6. 15	2	· C81, C85(12p→13p)		
1988. 8. 9	3	· R97, R98, R185, C63 삭제 · M1(MC82-VZ3603)→ MDLC3E383A · SW1(KSA-2228)→ KSA-1219		88-EE-140 PCB REV.C
1988. 8. 16	4	· VR2(220Ω → 330Ω)		88-EE-223
1988. 9. 20	5	· SW1, SW2(KSA1219 → JSS12065060)		88-EE-269
1989. 1. 6	6	· C65, C66(22p → 36p)		

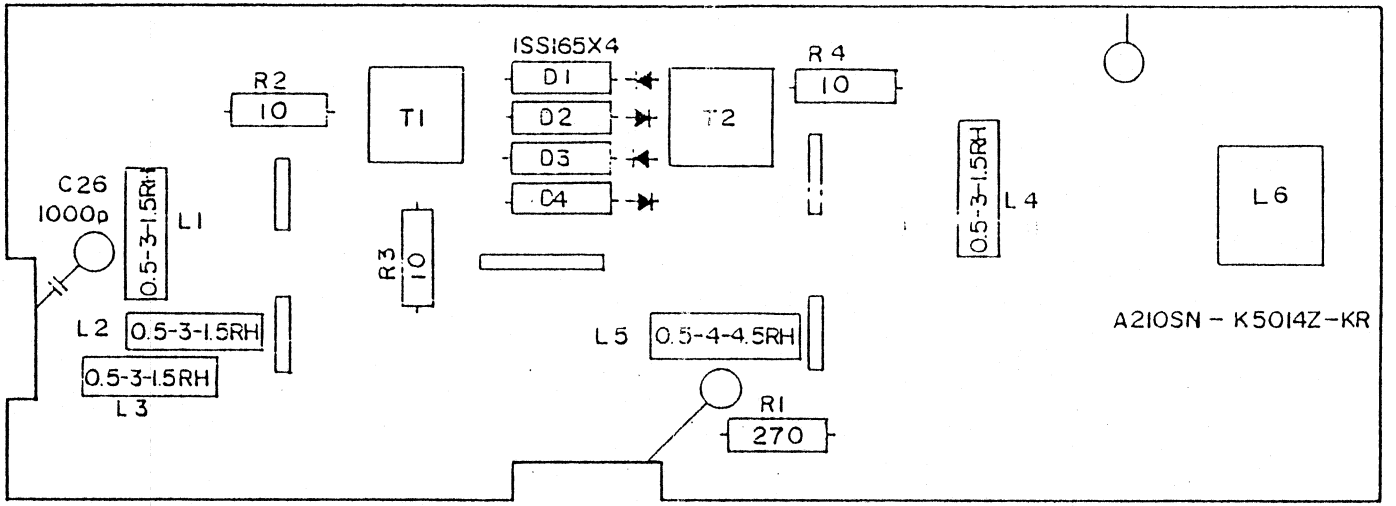
NOTE ;

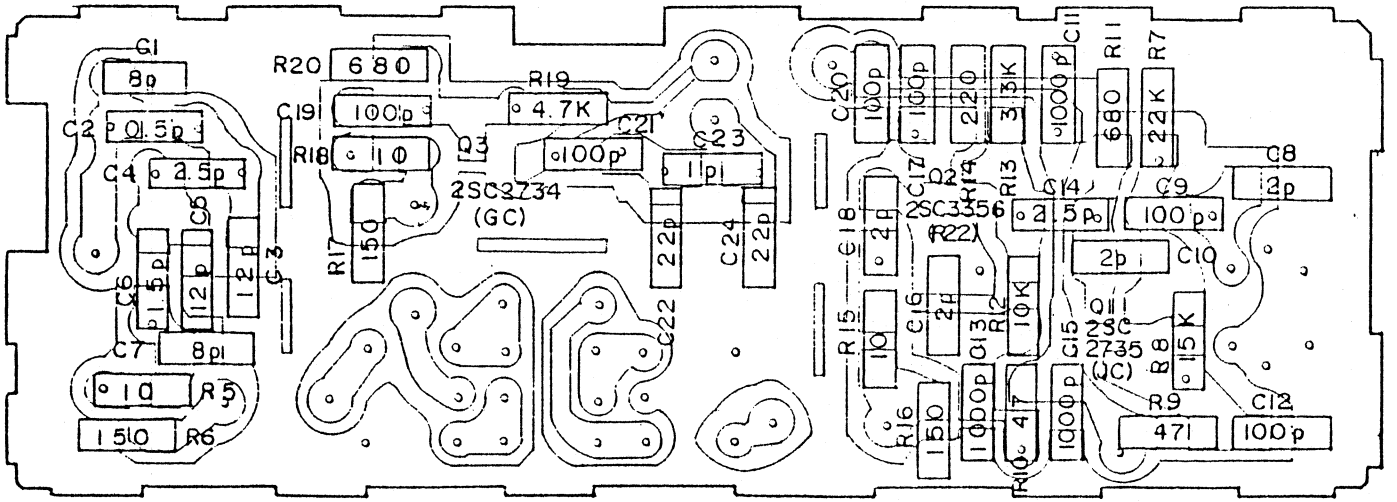
1. VR1, VR2, VR4, VR6 는 미조정 부품
2. P102-4 와 P108-4 JUMP(COAXIAL CABLE)

ECHOSTAR

SR-4500

Diagram 18: Main Printed Circuit Board

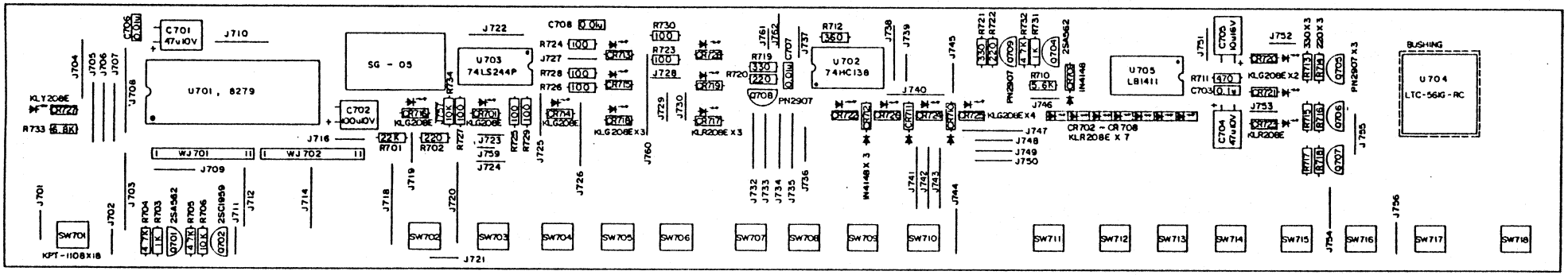




ECHOSTAR

SR-4500

Diagram 19: Second Downconverter PCB



NOTE ;

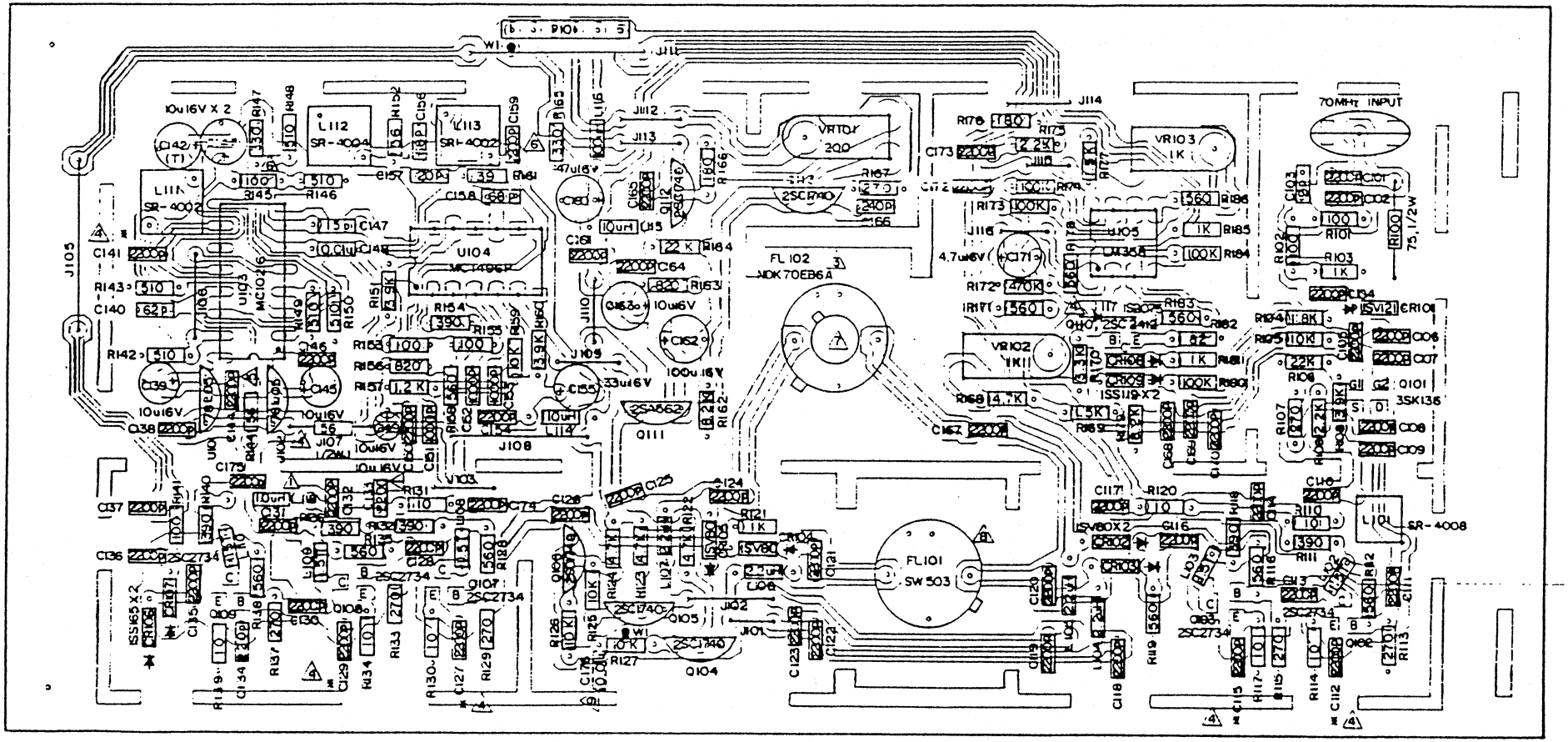
1. PCB 型號 Q703, R707, R708, R709, J713, J715, J717 J758 是

ECHOSTAR

SR-4500

Diagram 21: Front Controller Panel PCB

88. 7 29	7.8		88-[illegible]-95		3	J117 (1S2075) J107 (56.1/2WJ)		
89 5	9	C176 (0.01u) 추가	89-[illegible]-2002				87. 4. 25	1	J104 – L118 (10uH)	
88. 5 30					5	R144 (22,1/6W → 56)	88-[illegible]-015			
88. 2. 8					6	R161 (56 → 39) R145 (100, 1/6W)	88-[illegible]-029			
88. 2. 11						C142 (ELECT → TANTAL) C140 (43p → 62p)	88-[illegible]-033	87. 6. 15	2	FL102 (SBL0725 → NDK70EB6A)	
88. 5. 24						R175 (100K → 2.2K) R176 (8.2K → 180)	88-[illegible]-115	87. 11. 16	4	C112, C115, C127, C129, C141 (2200p) 추가	87-[illegible]-220



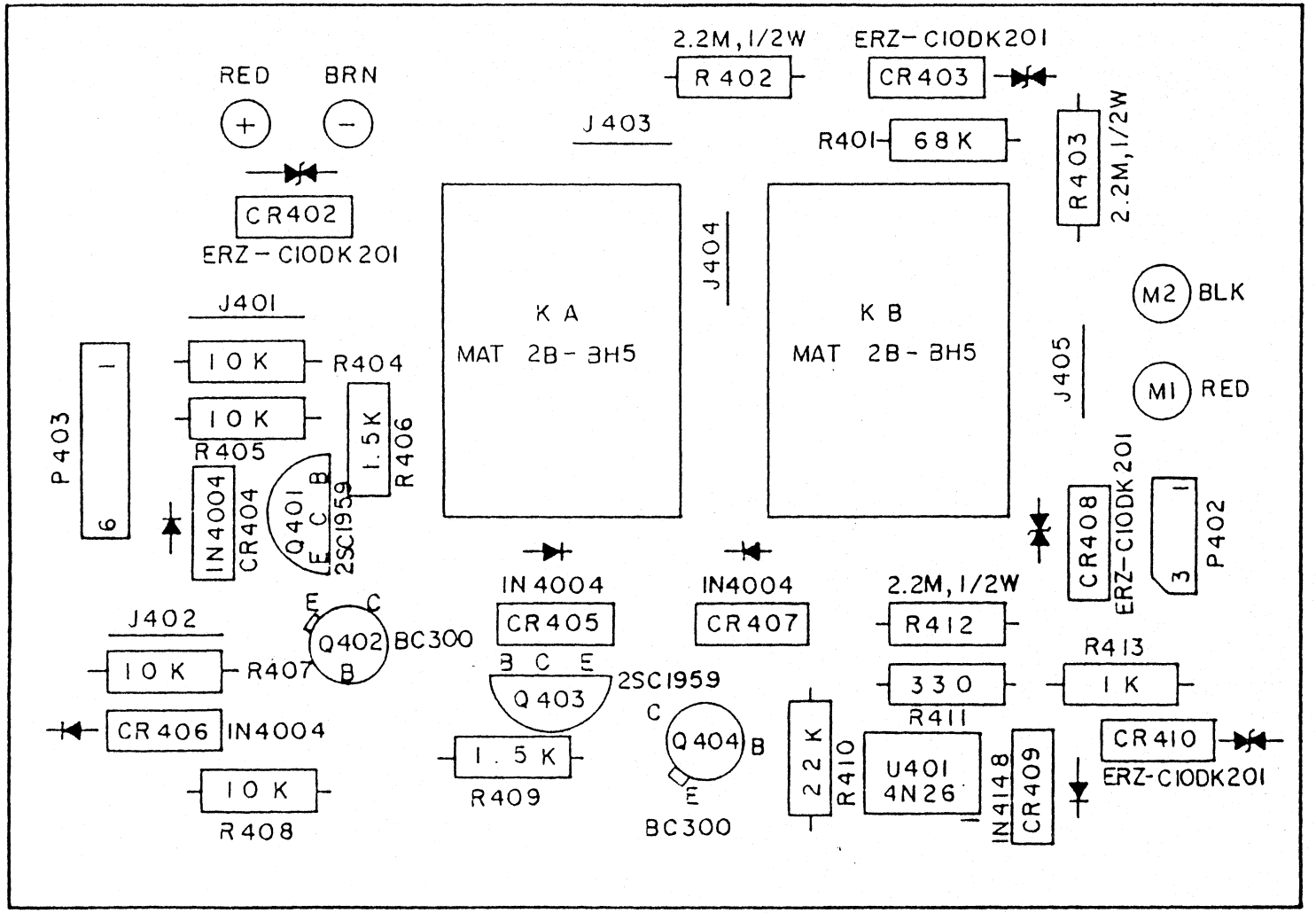
NOTE;

2. J107 : 56Ω 1/2WJ
3. J117 : 1S2075
4. * C112, 115, 127, 129, 141(2200p) : CERAMIC CHIP CAPACITOR,
5. R144 : 56 , 1/6WJ CARBON FILM
6. R145 : 100 " " "
7. FL102 : SBF0722 M 경로 SMALL FLAT
8. FL101 : SBF0731 R 경로
9. C176 : CERAMIC CAPACITOR

ECHOSTAR

SR-4500

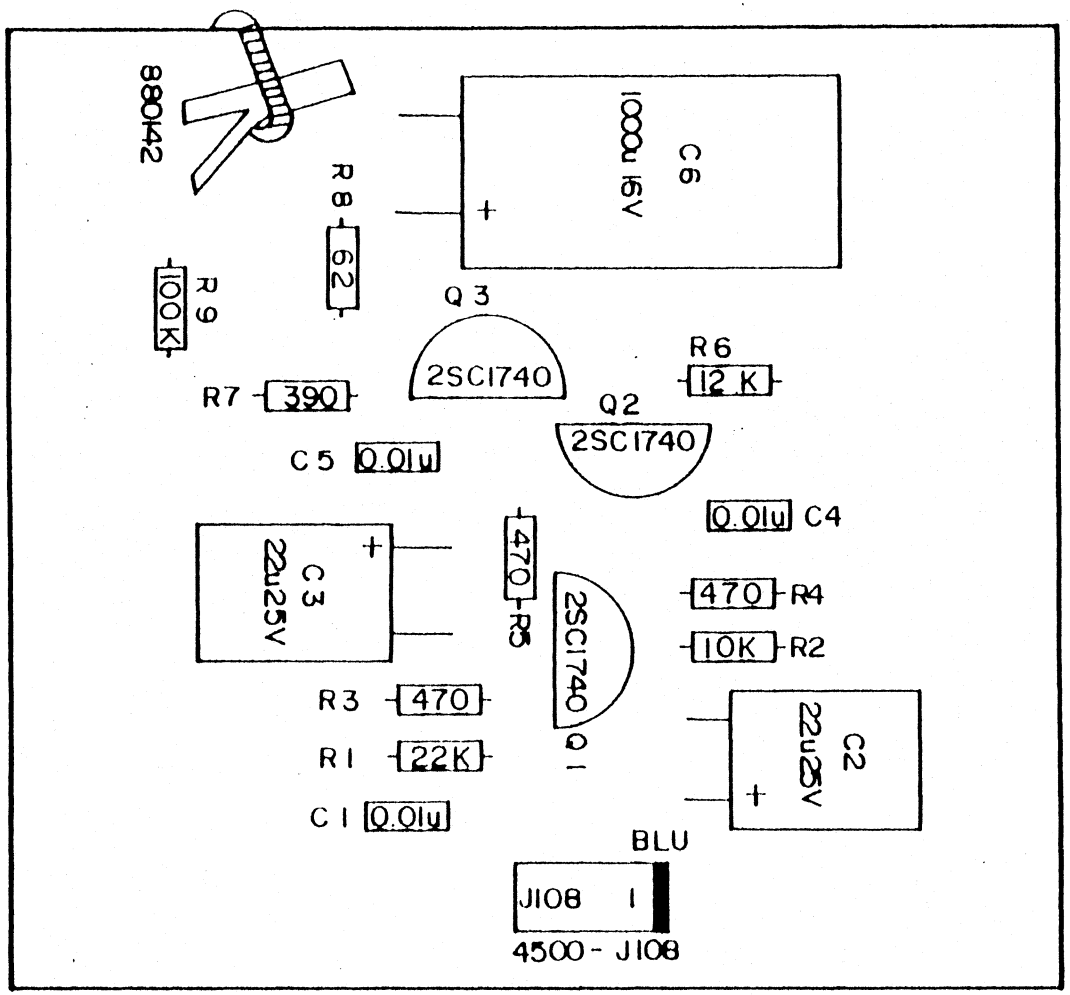
Diagram 20: Demodulator PCB



SR-4500

Diagram 23: Actuator Control PCB

ECHOSTAR
SR-4500
Diagram 22: Remote
Control PCB
C2002
100p
C2003
100p
220K
R2002
220K
R2003
Y2001
455KHz
U2001
6122G002
CR2001
FL-1L2
Q2001
2SC2710S
R2001
1.5, 1/4W
C2001
47u10V
+
-



ECHOSTAR

SR-4500

Diagram 24: MAC Amplifier PCB